Digital Circuits
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Lecture - 29
Sequential Circuits
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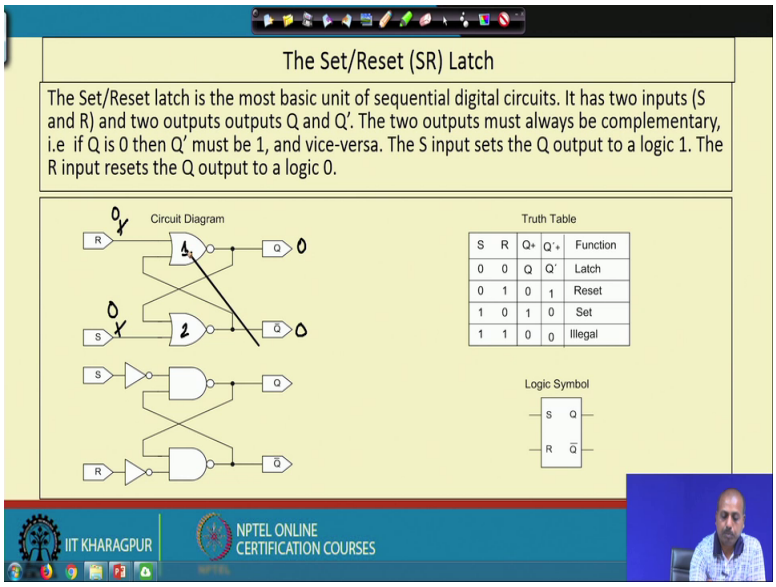

So, in the S R latch we have seen that the combination 1 1, we have said that this is illegal. So, why is it illegal? So, suppose we give this particular value say sorry, if we give this particular value say 1 1 then you see by; since these are simple nor gates, so you will get straightway 0 0 there fine now suppose after giving this after giving this 1 1.

So, we change this 1 1 to the values 0 0 we change both of them to 0 ok. So, we number these gates as gate number 1 AND gate number 2 ok. Now what happens is that so suppose these gate number so what is the. So, this is I have applied 1 1 so this is 0 0 and then I am applying here 0 0 and this is gate number 1 this is gate number 2 now suppose.

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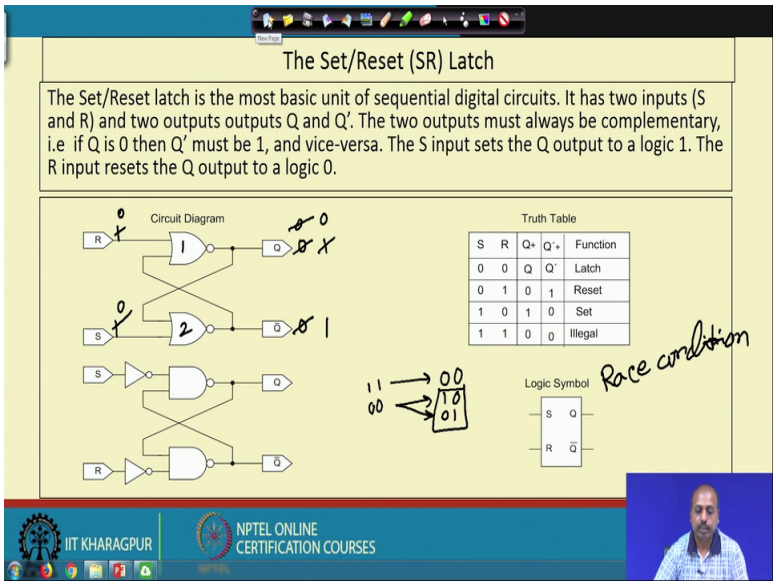

So, suppose I am looking into gate number 1, then what happens is that it both the inputs are 0 as a result this output becomes 1 and then this lower gate, so this case 1 input is 0 another input is 1 so nor gate, so these value remains at 0. So, it says that after the pattern 1 1 if so 1 1 gives me the 0 0 after that if I apply the input pattern 0 0 I am getting the pattern 1 0, but is my answer correct ok. So, to see that; so let us now consider the gate number 2 first; so this was so this was at a value 0 0 both the outputs were at 0 and then we consider gate number 2 first, then getting 0 0 so this will make this 1 as 1 and getting this 1 and 0.

So, this will make this 1 as 0 so that means, another possibility is from 0 0 it can also give rise to 0 1 and that is the problem that is the problem; you see if you apply 1 1 ones ok, then after that if you whatever pattern you will apply. So, this gate number 1 AND gate number 2, so they will race with each other whichever gate makes the transition fast and accordingly the output will be determined.

So, you see that in case of this gate number 1 AND gate number 2, so physically they are made on the silicon. So, they are not exactly of same speed ok. So, what will happen is that 1 of them will be faster than the other, but we do not know which 1 is faster that it is not possible to determine. So, we cannot say which transition will take place first gate number 1 transition OR gate number 2 transition.

So, as a result we cannot say whether the circuit will go to the output 1 0 or 0 1. So, this is the problem and this particular problem is known as the race condition. This particular problem is known as the race condition, as if the 2 gates 1 and 2 they are racing between each other to make the transition first. So, which ever gate means so sets the output to 1 ok.

So, that is the problem now with this so the that is why whenever we using S R latch, so we should we should be careful that we do not apply this pattern 1 1 to it see if we apply 1 1 both the outputs will become 0 so that part is fine if both of them are strong zeros, but after that the circuit behavior will become un predictable. So, as the gates will start racing between each other to make the transition, so we should avoid giving 1 1 to S R latch.

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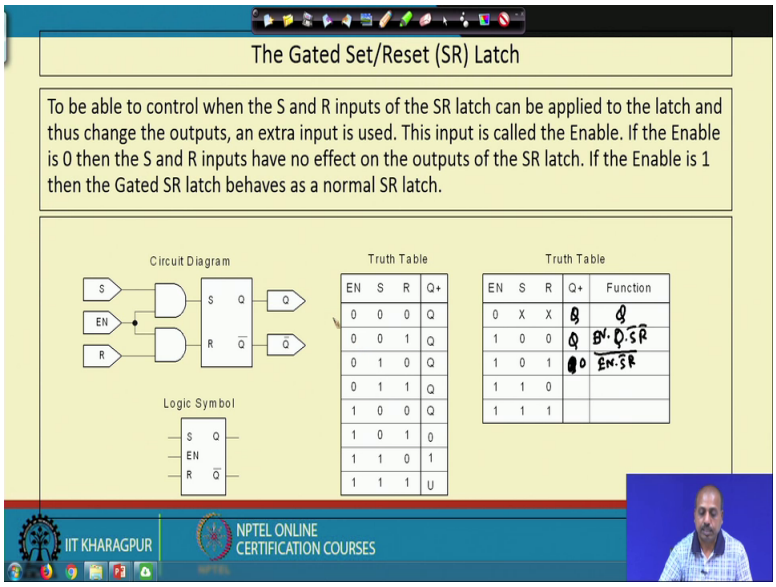

So, there is we can think about some enable signal. So, this they are known as gated S R latch, so to be able to control when the S and R inputs are S R latch can be applied to the latch. And thus, change the outputs and extra input is used so this is the enabled signal. So, this if this you can understand that if this enable is equal to 0, this if the enable is equal to 0 then both these S and R so this AND gates are getting 0. So, in case of in case of AND gate in case of S R latch so if you give 0 0. So, you see the circuit output does not change so they Q and Q bar they hold their previous values.

So, if I have this enable line so if this enable line is 0 so whatever values we give to S and R, so these 2 inputs will get 0 0 as a result Q and Q bar will maintain their previous values. Whereas, if we if we take this enable signal to be equal to 1 we take this enable signal to be equal to 1, then this S and R whatever values are coming so they will be coming to this S and R input and accordingly the circuit behavior will be determined.

So, we can say that so the a detailed truth table can be like this so in enable is 0 S and R being 0 0 0 1 1 0 or 1 1 so they will maintain the previous value Q and whenever this output is equal to whenever this enable line is equal to 1. Then the behavior will be determined by the then the behavior will be determined by this S and R inputs ok.

So, for example in this particular table so you can see that this when whenever this enable is equal to 0, so this is this will be holding the Q value. So, function is equal to Q and then whenever it is 1 0 0, then you know that the S R latch it does not changes it is state. So, that is equal to Q and this 0 1. So this is function is basically enable dot Q ok, then dot S bar R bar and then this function is again this is setting the this is setting this resetting the Q output so this is equal to 0.

So, we can say so this is output is the combination is enable then S bar and R and this whole bar because output is 0 in this case. So, this way we can finish you can write down this truth table or you can just make a carno map and try to figure out what is the function realized for this particular case.

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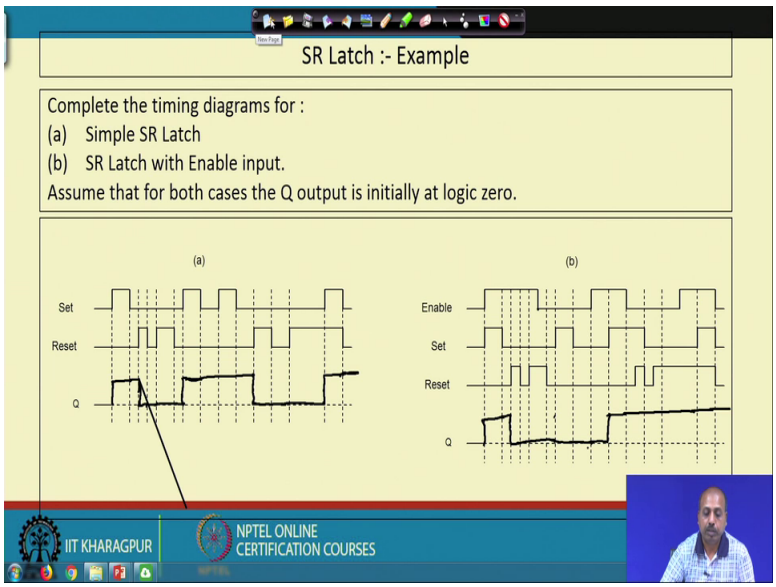

Next we will look into another example say this S R latch how will it look like, so I will urge you to finish this diagram. So, as it is said that we can say this is initially this Q output is low and here this S signal is going high. So, when the S signal is high the Q output will be high and then it will the after that S signal goes low this a S and R both are 0 0. So, 0 0 means it will continue holding the previous value and then the R signal is going high, so as a result so this will become low ok.

So, this remains low and then both of them are low so it will remain low then this R signal is again going high, so it continues to be low till this S signal becomes high. So, at this point S signal is high so this is going high and again. So, this is this is this will continue to be high till this R signal is becoming high so at this point R is high. So, this will be reset and then this will continue to be reset and then again at this point S signal is high so it will be going high.

So, it will continue being high because a S and R both have become 0. So, this way you can you can trace through this diagram. So, in similarly in this case everything remain same only thing is that the enable line also has to be considered. So, at this point enable is high and set is high as a result the signal will become high. And after sometime so enable is high up to this point, so till this point whatever changes are occurring in S and R so they will be considered.

So, it will come up to this point then this it will go down then again the S signal is high at this point, so it continues to be going like this and then at, but at this point it cannot change because enable is low. So, next enable is high at this point so up to this point the signal value Q value will be low and then when the enable is high the set line is going high at this point. So, this will become high and then again it will be then after sometime enable has become low.

So, it will continue like this and at this point enable become has become high active again, but here the S signal is again high so it continues like this. And then after this point enable signal is becoming low so it will continue like this. So, this way you can try to draw the diagram for this timing diagram for this Q S R latch operation ok. So, you just need to follow the truth table.

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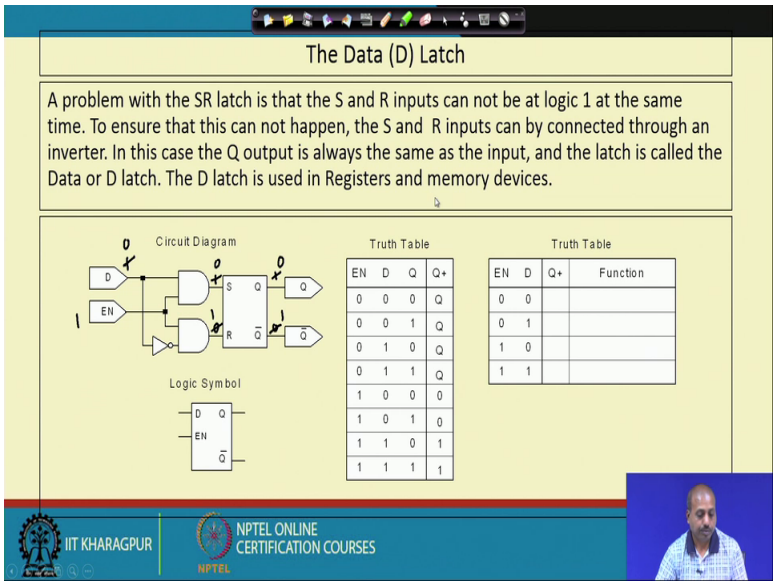

Next we will be considering another latch which is known as the D latch. So, D latch so essentially it this logic symbol is like this so it has got to 2 inputs 1 D input and 1 enable input; whenever D whenever this enable line is high whatever is coming in the D input will be copied on to the Q and Q bar is definitely the compliment of that. So, you see whenever enable is low enable is 0 this Q plus remains the holds the value of Q so it does not change.

But when this enable signal is 1 then D whatever irrespective of the value of Q the value is copied on to Q plus, so it does not depend on the on the previous Q value so it copies this D value to this, otherwise it will be remembering the if the enable is low it is remembering the previous value of Q, but if the enable is high. So, it is copying the current D value to the Q value so it is going like this. So, this particular latch this D latch can be realized by just connecting an inverter between S and R inputs of this of this S R latch.

So, you see that in case of in this case what is happening is that if I apply a so enable I am taking as permanently 1, now if I give D equal to 1 then what will happen so this S will come as 1 and this R will come as 0. So, as a result this Q output will be set to 1 and Q bar will be set to 0 that is from the behavior of S R latch. Now if I do if I put D equal to 0 and this enable equal to 1 then this is 0 and this is 1 and by the behavior of a S R latch we know that it will reset this Q output to 0 and Q bar to 1. So, you see if we make

an S R latch and we just connect and inverter between this S and R inputs. So, we get the D latch and here of course there is no S R around condition because, in into if the in our S R latch so it never gets this both S and R inputs as 0. So, both S and R inputs as 1 so as a result the S R around condition is not there say you again finish of, you can complete the truth table for the S R for the D flip flop not doing it now.

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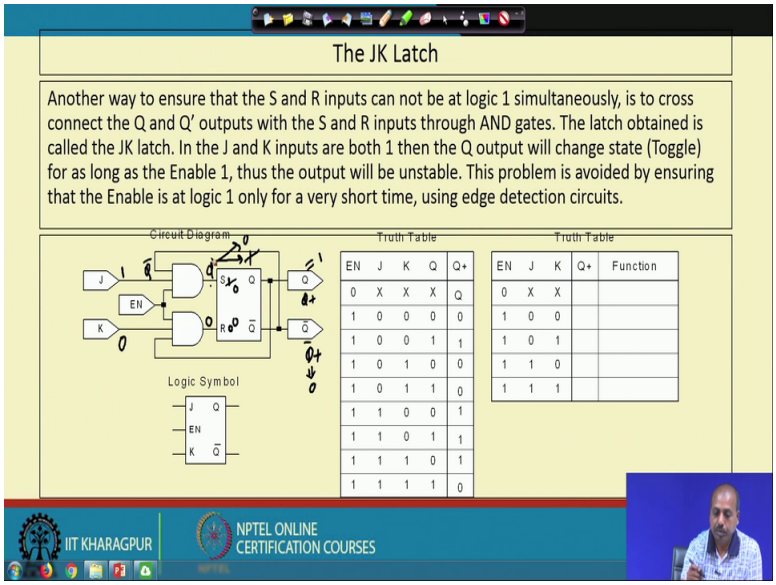

Another interesting type of latch that we have is known as the J K latch, so in case of J K latch what is done is that it is a 2 input it is a 2 input circuit. So, J and K these are the 2 inputs and it has got a third enable input. So, when this enable line is 0 by our definition we know that whatever be the values of this J and k. So, it will continue to the latch will continue to hold the previous value of Q, but when this enable line is 1 then the behavior of the system will get affected how.

So, this is 1 way to ensure that S and R inputs cannot be at logic 1 simultaneously is to cross connect Q and Q bar outputs with the S and R inputs through AND gates what is done this Q bar line is taken back and it is this it is fed as an input to this AND gates. So, this AND gate it has got 3 inputs. Now J Q bar and enable and then this K it has got inputs like this Q this Q line is coming here. So, K Q and enable so these 3 are put into this AND gate and they are put into this S R latch input.

So, so the type of latch that we get is known as the J K latch now otherwise, so when there is a behavior is almost similar to the S R latch like if I have this say J equal to 1 and

K equal to 0. So, what will happen is that this R input will be equal to 0 and then this and then this Q bar line is coming here Q bar line is coming here so this gate is the Q line.

So, Q may be equal to 0 or may be equal to so, so this is a previous Q ok. So, this is the previous Q so this Q if I say if I write it as Q plus and Q bar plus that way. So, what have what happens is that so this previous Q plus Q bar was coming here so that is ANDed with J equal to 1. So, it get a previous Q value coming here now this Q there are 2 possibilities this Q may be equal to 0 or this Q may be equal to 1. Now if this Q is equal to 1 in that case this case input is 1 and R input is 0 as a result this S R latch will be set.

So, this Q bar Q plus will become equal to 1 and Q bar plus will S become equal to 0, on the other hand so if the Q value is equal to 0 if the Q value is equal to 0 then what you are getting is you are getting a 0 here and 0 there, as a result this Q it will be maintaining it is previous value. So, you see that when these J input is 1 so this when this J input is 1 then if this Q value is 0 if the Q value is 0 then it is going to sorry here it is here it is Q bar is coming I am just explain it once more.

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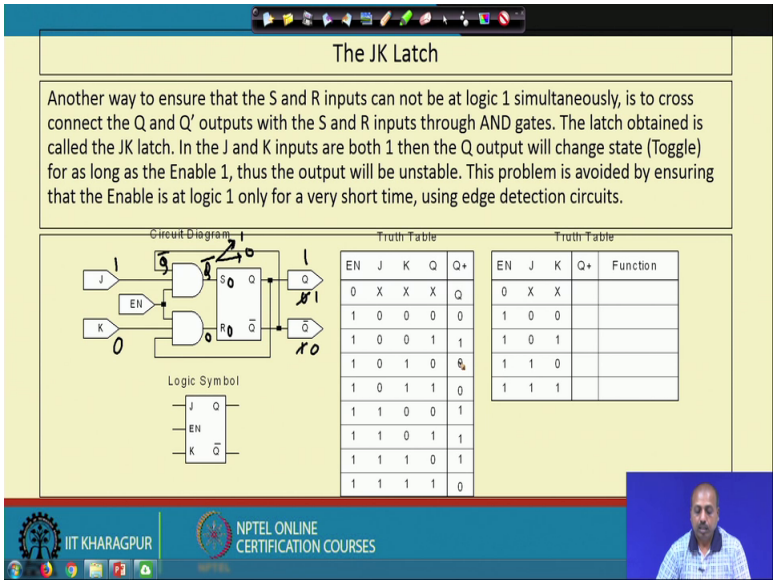

So, I said J equal to 1 and Q equal to K equal to 0 and this so this Q bar line is coming here, so this Q bar line is coming here. So, this Q bar can be equal to 1 or can be equal to 0 this line is 0 there is no problem. Now if this Q bar line is equal to 1 in that case this Q line was previously it was 0 Q bar line was 1 now, because this is this is S R latch and this Q input this S input is equal to 1, so this will set it to 1 and this will go to 0. On the

other hand if this Q bar line was 0 ok, that means this Q line was equal to 1, so it will continue to hold the value 1. Since I am getting a 0 0, here so it will continue to hold the value 1.

So, in case of J K flip flop what J K latch what happens is that if you give this J and K J inputs as 1 and K input as 0, then irrespective of the previous value of Q the new value of Q becomes equal to 1 and you can also trace the other way that is if the K value is K is made equal to 1 and J is made equal to 0 then irrespective of the previous value of Q, so it will become equal 2 0; so Q plus will become equal to 0.

So, that way it is behaving more like a S R latch, but only thing is that that racing condition cannot occur because a illegal combination cannot be applied. Of course, there is another issue like if I make this both this J and K equal to 1, so I make this J and K both of them equal to 1.

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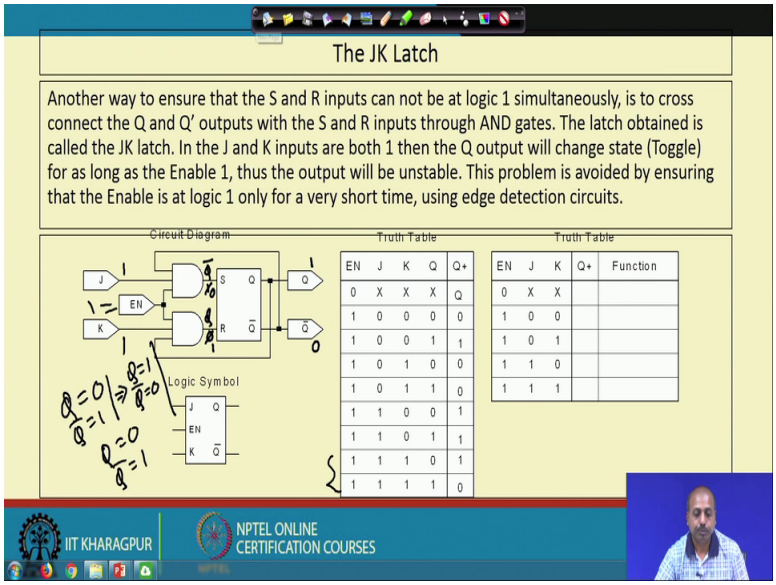

So, what happens is that this Q line comes here? So Q line the previous Q value will be coming here and the previous Q bar value will be coming here. Now suppose Q was equal to 0 Q was equal to 0, so this is equal to 0 and this is equal to 1 as a result this line will become 1 and this line will becomes 0 ok. Now you see that after that what will happen after that this 0, so I had Q I had Q equal to 0 Q bar equal to 1 from there it has gone to a situation where Q equal to 1 and Q bar equal to 0. Now then what will happen this 0 will be coming back here so this will make it 0 and this and this 1 will be coming

back here will make it here equal to 1 and by the S R latch property next time what it will do it will make Q equal to 0 and Q bar equal to 1, it will reset the latch and so it will make Q equal to 0 and Q bar equal to 1.

So, what is happening is that this will go on happening continually. So, if this as long as this enable line is equal to 1 if J and K both are made high then this latch so it will go on toggling the states. So, once this once it will be equal to 0 and then it will become equal to 1 and that will happen continually. So, this is a explained in these two rows like, if this enable is 1 then if J and K both are 1 then if the previous value of Q is 0 now the value will become 1 and since the enable is 1. So, now what will happen is that this 1 will come here as a result it will again change to 0. So, the Q line will continually flip and this Q bar line will also continually flip, so this is the problem with the J K latch that as long as this enable is equal to 1 output will be unstable.

So, this J K J and K inputs are both 1 then Q output will change state for as long as the enable equal to 1 and the does the output will be unstable. The problem can be avoided by ensuring that enable is at logic 1 only for very short period of time by using some edge detections circuitry.

So, this type of if the problem with this circuit is that is as long as enable signal is high, so it is thus whatever values in J are coming in J and K so they are taken into consideration. So, if we can do something so that this enable is not high for a significant amount of time only for a very small amount of time it is active. So, we get we go from this level triggered circuit to edge triggered circuit, then for the edge triggered circuit this type of problem will not occur anyway we will see that.

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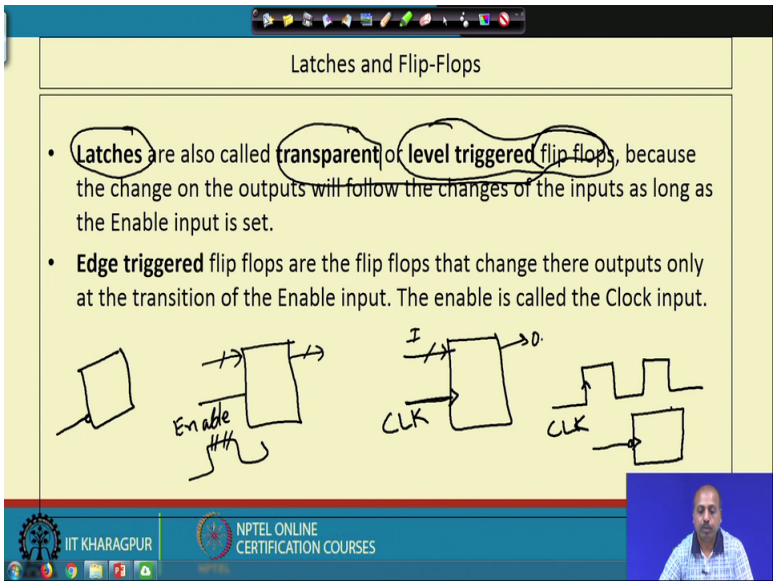

So, the latches are also called transparent or level triggered flip flops because, the change in the outputs will follow the changes of the inputs as long as the enable input is high. So, so far what we have what we have seen is that we have got if this is whatever S R latch S R D JK whatever it is so we have got an enable line and we said that as long as this enable signal is high. So as long as this enable signal is high whatever inputs are that is going to affect the output. So, these type of sequential circuits so they are known as latches or transparent or level triggered flip flop. So, these three terms are synonymous latch transparent flip flop and level triggered flip flops, so these three terms are synonymous.

So, latch transparent flip flop and level triggered flip flops, so these 3 terms are synonymous on the other hand see if we have some edge triggering. So, edge triggering means theses clocks this enable line or clock line whatever you call it. So we put a hat at the triangular shaped structure at the beginning and then whatever will be the input so that is coming. So, this is input output now this is so this means that we will be considering the input changes only at the edges of this signal ok.

So, whatever you call it. So, normally we call it a clock signal so this whenever this clock edges come. So, they will be considered so you can make you have got also symbols for this low level triggered and falling edge triggering. So, low level triggered so this is the represented by a diagram like this enable line we put a bubble at the end so

that is the low level triggered; similarly for this falling edge triggered flip flop, so this clock signal is shown like this the clock signal is shown like this so that is a falling edge triggered. Whereas, this one is a rising edge triggered so this type of notations are used for due to distinguish between different types of flip flops we have.

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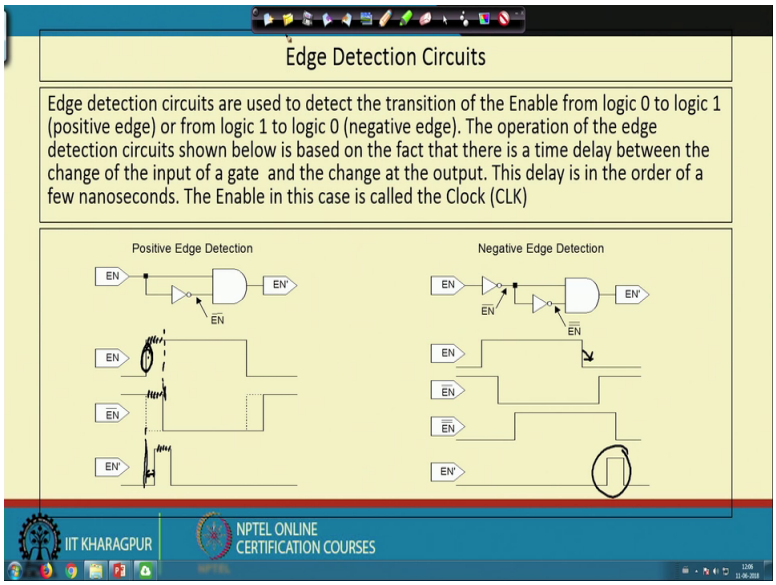

Next we will look into how to detect the edge so we have said that I want to detect the edge, but how to detect it. So, edge detection circuits they are used to detect the transition of the enable line from logic 0 to logic 1 or from logic 1 to logic 0. So, it can be done like this see suppose I have got this enable signal and we put an inverter and end these 2 signals, then what will happen if this is the enable signal it was low for this much time now then it is became high and then again it is low.

So, you want to detect this situation that when the transition occurred from low to high. For detecting that situation we put an inverter so due to the delay of the inverter this EN bar signal, so this will be delayed by some amount of time ok; so this is delayed by some this much of time. Now if you take this AND gate then what will happen this so this output of AND gate will be high only for this small amount of time. So, this is not so if you considered the delay of and get also.

So, you see that so for this much for this period of time both the signals are high ok. So, that will be coming to that that comes to the output of the AND gate so that corresponds to this much time and it is slightly time shifted and that delay from here to here. So, this

is due to the delay of the AND gate, but anyway so by using this circuit. So, I can detect the precise time at which this transition has occurred from low to high, similarly if you are going for to detect high to low transition then we can go we can make the circuit like this, so this enable line is inverted and then another inversion.

So, that comes like this and then if you go on doing this ending you will see that ultimately it will land into a pulse on this line when the which actually corresponds to this transition this high to low transition, so this corresponds to this transition. So, this way we can use these digital gates to realize this edge detection circuits, and then use that this EN EN dash signal as the edge triggering clock signal for the flip flops.

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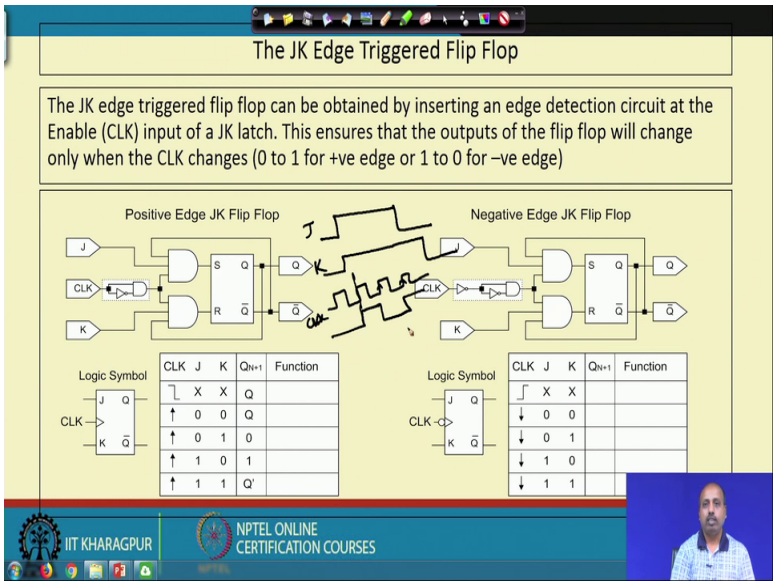

We will next look into edge triggered J K flip flop. So, this edge triggered J K flip flop, so as I said that edge triggering can be positive edge triggered or negative edge triggered. Now you see that this circuit is otherwise similar to whatever we have seen this previously we this name of this line has changed from enable to clock otherwise the lines are same.

So, previously so this line was drawn directly and connected here, now we have put a small edge detection circuitry between before this. So, that way we are we have done it like this now what happens is that this only during the time for which this line is high and that precisely happens when the clock is making a transition from high to low. So, only when this making a transition from high to low sorry, when this transition is low to

high like this then only this output will be equal to 1 and then only this J and K values will be allowed to come to this is S and R. So, whenever this clock is high or clock is low or clock is making a transition from high to low. So, this output at this point will be 0 as we have seen in the previous slide, so you see that when only when this was making a transition from low to high. So, this pulse came otherwise this e n dash line was always 0, so this following edge was not detected here.

So, that is why so if it is a falling edge or high level or low level of the clock signal with respective of the values of J and K this Q will maintain it is previous value; whereas, if there is a rising edge like this then this depending upon the value of J and K this Q the Q value will change. So, it will be becoming equal to 0 or 1 or either it will maintain it is previous value or it will be changing.

Now because of this edge triggering so we cannot have the we cannot have these toggle because, this by the time this toggle if the toggle has to occur then this clock has to appear again this clock transition has to appear again and for that we do not bother. Because, in the previous case what was happening is that you will be depending upon the delay of this J K flip flop, depending upon the delay of this gates so this is S and R settings where being done.

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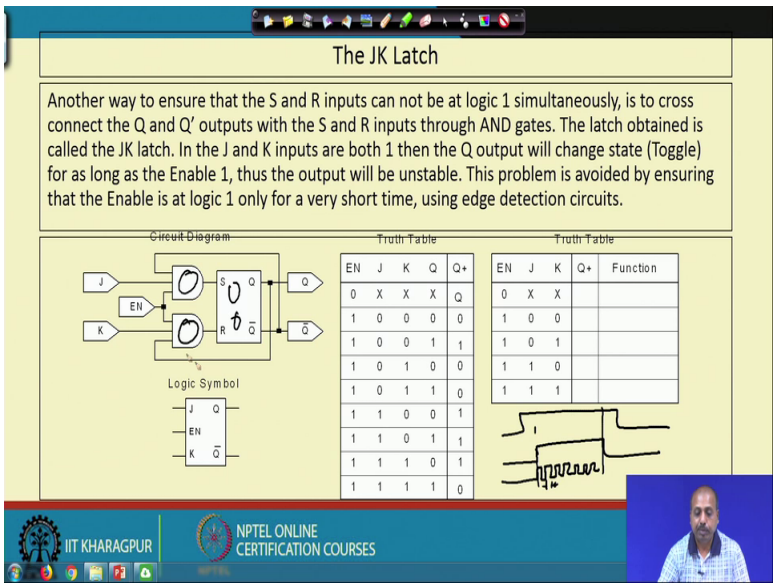

So, what was happening is that: so if this J is high for this much of time and K is high for say this much of time, so during this time this Q output will be continually changing like

this Q output will be continually changing like this. So, why this thing happens so this particular delay is equal to the delay of this gates this, the AND gates and all and this the NAND gates or NOR gates that we have inside. So, this is determined purely by the combinational elements that you have in the circuit; whereas, for the edge triggered circuit so we are not we will be getting this type of behavior, but only at the clock boundaries.

So, that is why we are we are it is much safer, like here also if the J and K both the signals are high if J and K both the signal are high like say J is high for this much time and K is high for this much time. Now in between if you have the clock signal going like this so this is the clock then the transitions you will see the Q bar Q output is so at this point the Q value will change the Q was Q will change here. Again at this point at this point the Q will change again at this point Q will change, so that is determined by the clock boundary.

So, it is controlled it can be controlled externally by controlling the clock signal you can control the toggling rate whereas, for the latch JK latch we do not have that control, so that is purely determined by the delays of the constitution gates in the latch. So, this J K edge triggered flip flop it solves that toggling problem and that way it is helpful.