Low Power VLSI Circuits and Systems

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Lecture No. # 08

MOS Inverters - III

Hello, and welcome to today's lecture on MOS inverters. Today, we shall discuss about the switching characteristics of MOS inverters of course, before that we shall be discussing about the various types of MOS inverters that we have discussed in the last two lectures and we shall have some kind of comparison.

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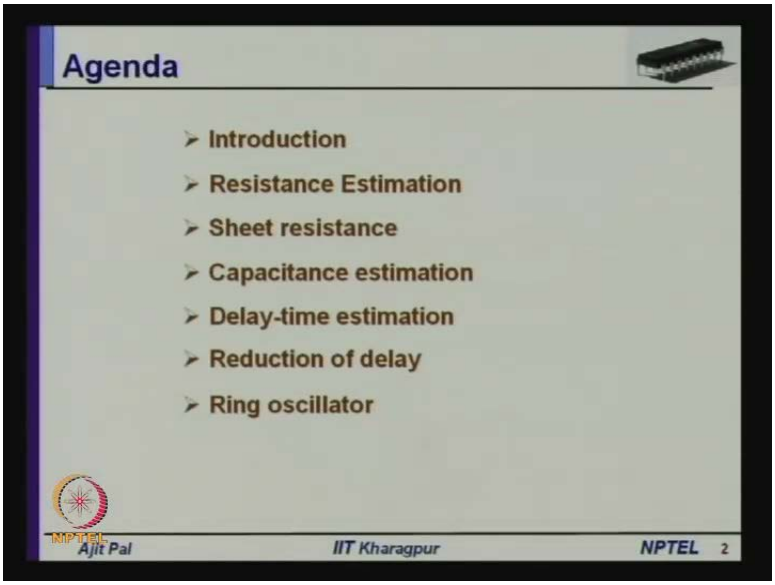

And here is the agenda of today's lecture. This is primarily on switching characteristics after giving brief introduction we shall discuss about the resistor estimation. We will see that different types of resistors are present in a V L S I circuit and that resistor will lead to some delay, because you know the resistance and capacitance these two are the parameters which are responsible for the delay of a circuit. So, we shall discuss about the resistance estimation how we can estimate the resistor then capacitance estimation then we shall discuss about the delay time estimation in terms of the resistors and capacitors,

then how we can reduce the delay various techniques which you can adopt to reduce the delay that we shall discuss and another technique we shall use to measure the delay with the help of ring oscillator. So, these are the topics we shall cover, but before that.

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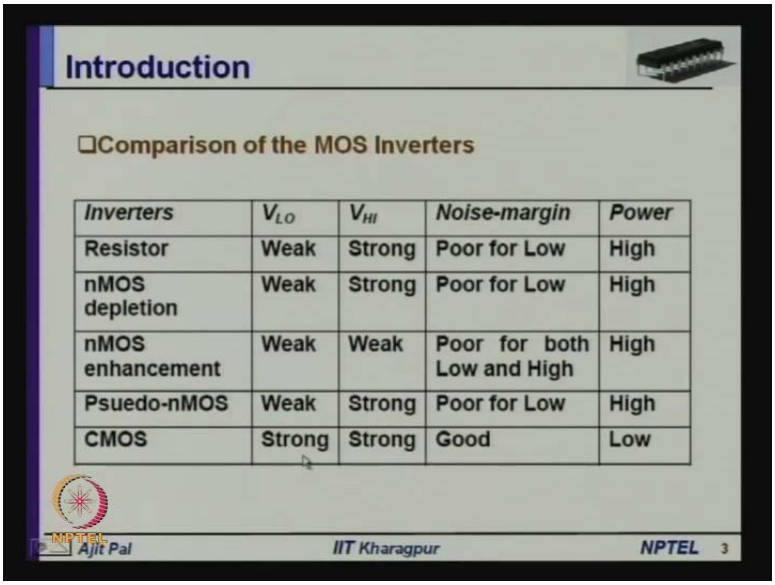

Let us have a comparison of the MOS inverters. So, in the last two lectures we have discussed different types of inverters MOS inverters that you can realize. We have seen the resist the inverter is realized with a nMOS transistors as the pull down device and various type types of pull up devices like, resistor nMOS depletion mode transistor, nMOS enhancement mode transistor, pseudo nMOS transistor, I mean inverter that is actually p type nMOS transistor that is use as pull up device then CMOS inverter.

So, these are the various types of inverters we have discussed and these are the 4 parameters which we shall compare one is your V LO. V LO is essentially the low level output Voltage of the inverter; that means, when the output is supposed to be 0 V OLt low level then whatever Voltage it provides that is represented as V LO and we can see for all the inverters except CMOS the V LO is weak the reason for that is very clear.

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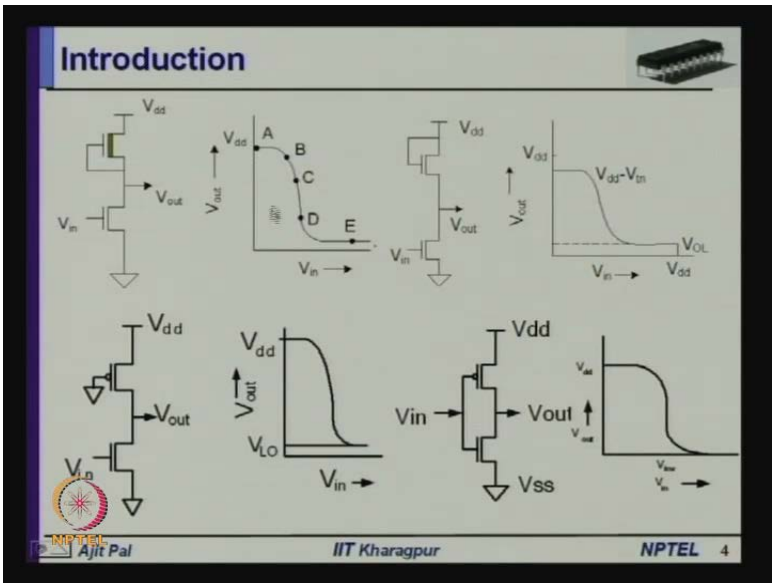

From these diagrams you can see here the, this is this is the case for depletion mode transistor is pull up. This is the case for enhancement mode nMOS transistor is pull up and this is case for pMOS transistor is used as pull up and this is finally, this CMOS using pMOS transistor is pull up. So, in all the cases we find the v low is above 0 level here, even for pseudo n MOS, but in case of CMOS it is you are getting 0 for 0 level. So, that is reason why you can see the only for CMOS the low level is strong means you are getting ground level output, when the low level Voltage is 0 for all other cases it is weak because the is that you are getting little higher than 0 V OLt at the output.

Similarly, reason we can compare the high level output which is strong for all the cases except for nMOS enhancement type inverter, I mean where the pull up device used is nMOS enhancement type for all other cases, it is strong means here getting V dd. We shall be getting V dd at the output as you can see from these diagrams we are getting V dd when we are using nMOS depletion type transistor as pull up we are getting V dd minus when pMOS transistor is used as pull up and in case of CMOS also you are getting V dd at the output, but in case of nMOS enhancement type transistor is pull up we are getting V dd minus Vtn as the high level. So, we can see here except for nMOS enhancement type inverter I mean where enhancement type transistor is used as pull up device, we get strong v d t then consider the we have consider the parameter noise margin.

So, we have seen noise margin is poor for low for resistor type inverter where resistor is used as pull up or where nMOS transistor is used as pull up or where nMOS enhancement type is used as pull up or for pseudo nMOS use device is used for all the cases noise margin in poor for low level. The reason for that I have we have already seen because we are getting a output which is above the ground level; obviously, noise margin will be inferior for low level, but for CMOS we are getting good noise margin because you know that we get low level output here. So, noise margin is good for C MOS, but we find that noise margin is bad both for low and high level in case of when the nMOS enhancement type device is used as pull up we know that the noise margin in…

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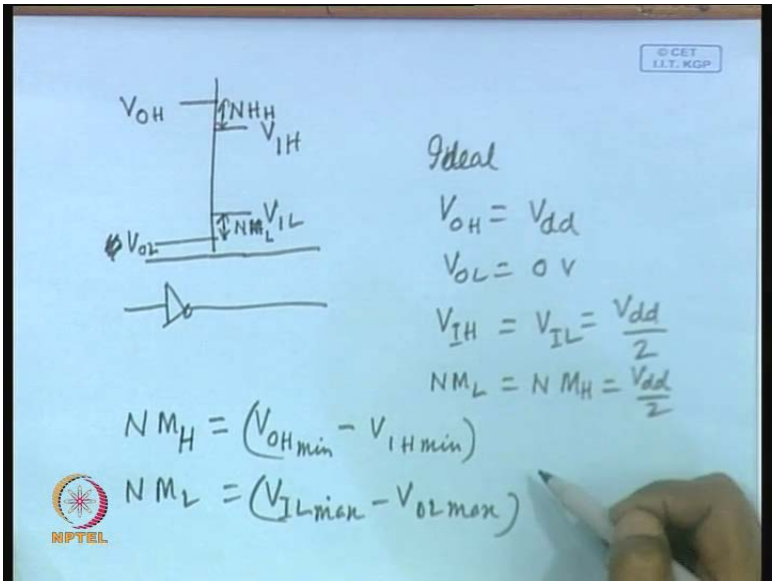

Let me emphasize the point here, we know that this is the V OH that is being generated by the device and similarly, V OL that that is generated by the device at the output say inverter is producing that. On the other hand we are expecting V IL at the output as long as it does not exceed that limit then we are getting we shall be considering that low level as low level similarly, V IH is the high level output.

Minimum high level output that is expected. So, this is the noise margin at high level and this is the noise margin noise margin at low level, so this particular. Now ideally as you know in case of ideal situation V OH should be equal to V dd V OL should be equal to 0 VOLt similarly V IH and V IL should be equal to V dd by 2; that means, transition should be should take place in the middle and both of them will be at V dd by 2 So, in

that case your noise margin for both low and high level will be equal to noise margin low will be equal to noise margin high both will be equal to V dd by 2, but we have seen that is not the case.

So, noise in reality noise margin low is defined as the V OH 4 H minimum minus V IH minimum similarly, sorry this is your V N M H similarly, that N Noise Margin low will be equal to V IL minus maximum minus V OL maximum. So, these are the actual noise margin and; obviously, it deviates from the actual situation that we have already discussed and we find that noise margin is good only for C MOS.

Then coming to the power dissipation the fourth important parameter is power we find that power dissipation there is power static power dissipation, when the power is low for all the cases except for C MOS. So, we have seen that in all the cases both the transistors are on both the transistors are on here, in case of this inverter weak enhancement mode transistor is pull up sorry or depletion mode transistor is pull up or enhancement mode transistor is pull up or pMOS transistor is pull up in all the cases both the transistors are on when the output level is low or when the input is high level and as a consequence there will be static power dissipation and power dissipation and; obviously, they are not suitable for low power application.

But in case of CMOS we have seen both for low level and for high level only one of the two transistors is on and as a consequence there is no static current flow and; obviously, there is no power dissipation when the output is low or when the output is high of course, as we have seen in case of CMOS there is power dissipation when input changes from 0 to 0; 0 to high. So, during the transition or from high to low, so, that part we get there, but that will be dependent on how quickly the transitions occur, later on we shall discuss about it in more detail, but as such there is no static power dissipation in CMOS except during transition. And as a consequence we find that the power dissipation in CMOS is low and from these comparisons what can we what conclusion we can make we find that all the 4 parameters that we have discussed is good for CMOS and that is the reason why CMOS is the technology of choice and CMOS is used for all recitative VLSI circuit realization and; obviously, they are most suitable for low power application because of low power dissipation.

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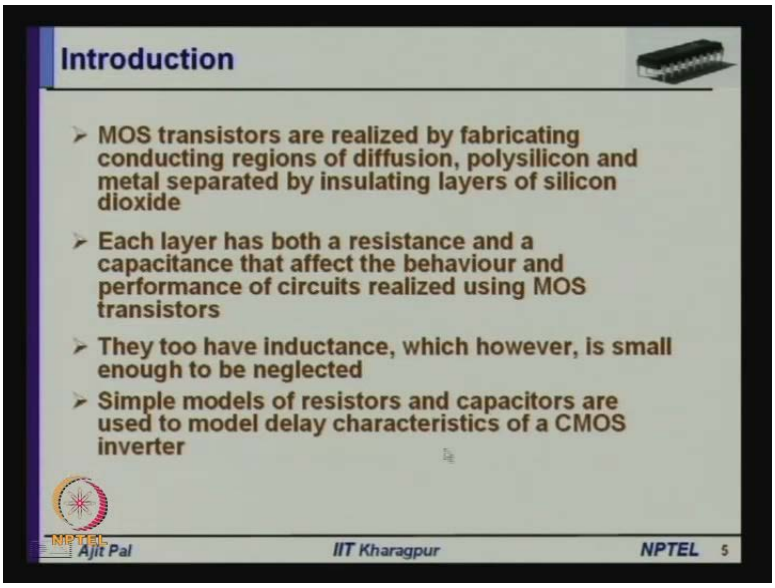

So, with this comparative study, let us move to our main topic that is your switching characteristics of CMOS inverters. So, we know that most transistors are realized by fabricating conducting regions of diffusion, poly silicon and metal separated by insulating layers of silicon dioxide that we have already studied in the first lecture itself and as we know each layer has both a resistance and a capacitance that effect the behavior and performance of circuits realized using CMOS transistors and obviously, these conducting layers will have finite resistance and also capacitance associated with them and that will affect the switching characteristics; switch characteristics means, when the input is changing from may be from low to high or high low output is also changing from high to low or from low to high.

So, that those will be affected because of the I mean resistance and capacitances of course, they too have inductance which; however, is small and enough to be neglected; that means, the inductance value is too small and obviously, they contribute very little in the operation of the switching characteristics I mean, they will not affect much the switching characteristics of the devices and that is the reason why we shall ignore the inductive power of the different components that we shall be using, we shall be mainly restricting to capacitance and resistances of the devices and; obviously, to start with we shall discuss about simple models of resistors and capacitors that can be used to model delay characteristics of CMOS inverters. So, you see now we shall focus only on CMOS

inverter or CMOS complex circuit we shall not discuss about any other types of inverters that we have discussed so far.

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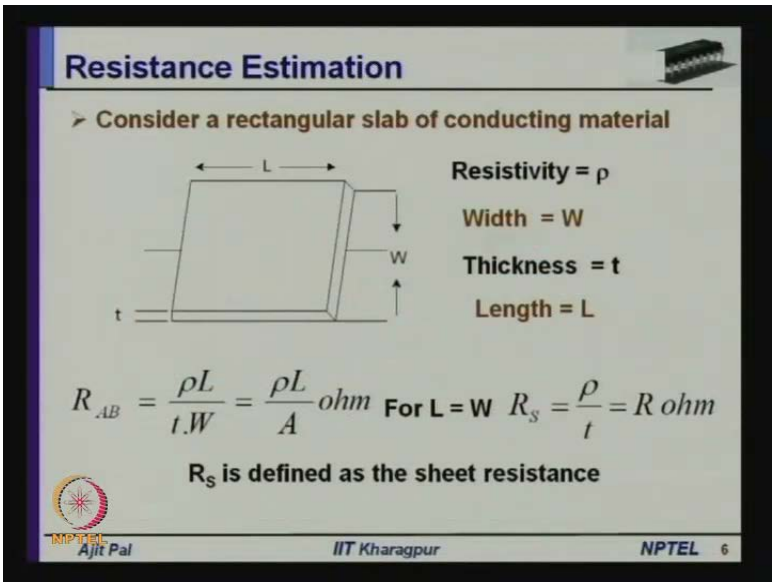

Coming to Resistance Estimation, let us consider a rectangular slab of conducting material let me draw it here, let us consider a rectangular slab of material.

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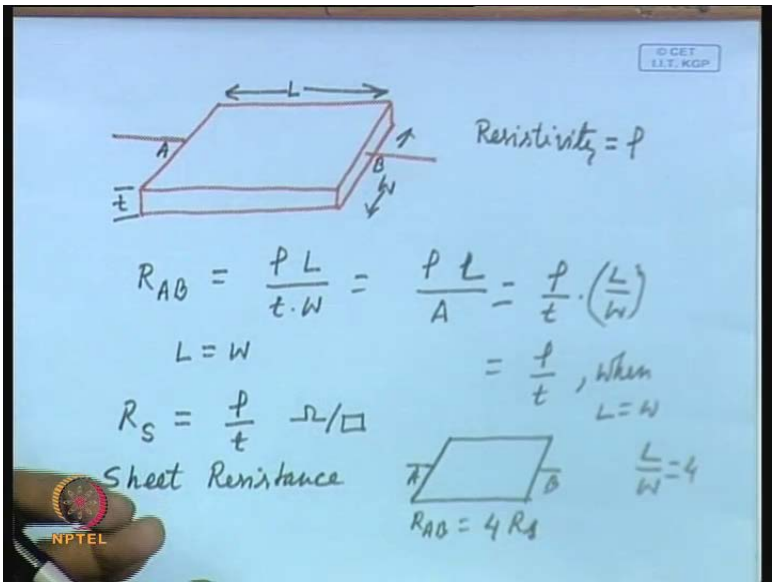

So, this is a rectangular slab I have drawn and we have one conductor on this side another conductor in other side for taking interconnection; that means, when we want to measure the resistance of this slab and by attaching a may be millimeter or some other

device at these 2 ends now the physical dimensions are shown here L is the length of the slab and W is the width of the slab and t is the thickness of the slab. And in addition to this it has got another very important parameter in the context of resistance estimation that is your Resistivity is equal to rho and rho defines the resistivity of the material that we will be using and; obviously, this resistivity will vary from mater from material to material we have seen we shall be using different types of conducting material like diffusion region poly silicon metal and. So, on and; obviously, their resistivity will be different for different material and.

So, if this we consider this point A and this point B this resistance between these 2 terminals A and B will be equal to rho L by rho L by t into W. So, this is the resistivity of the of this particular conductor between these 2. Now this can also be represented by rho L by A area is essentially the area of the device; that means, area will be equal to t into W that is the area and n is the length. So, based on this we can this can be also represented by another very important in another way say it is actually L area L by w. So, let us represent in terms of rho by t into L by W. Now let us consider a situation where L is equal to W; that means length is equal to width in that case it is a I mean it is square.

So, whenever it is a square that square can be one nanometer by o1 nanometer or 1 millimeter or 1 meter by 1 millimeter it does not matter because as long as these 2 are same they will cancel out and this will be equal to rho by t and when L is equal to W, then whenever this is a situation we define a parameter known as R S, R S is equal to rho by t and you need these ohm per square. So, an ohm per square is the unit of this seat resistance. So, this is called the seat resistance.

Seat resistance of the material point of an the resistivity of a conducting layer is specified in terms of the seat resistance the reason for that is using this parameter you can calculate the resistance for a given dimension for example, you are given a say this is the let us assume we are considering say we know that let us assume that L by w is equal to say 4 let us assume that L by w is equal to 4; that means, with L by W length by width is equal to 4 and what will be the resistance between A and B and obviously, in that case we can express it in terms of R A B will be equal to 4 into R S when L by W is equal to 4. So, you can see we can express the resistance of that particular layer in terms of the seat resistance, if we know the length and width of the device of a particular material.

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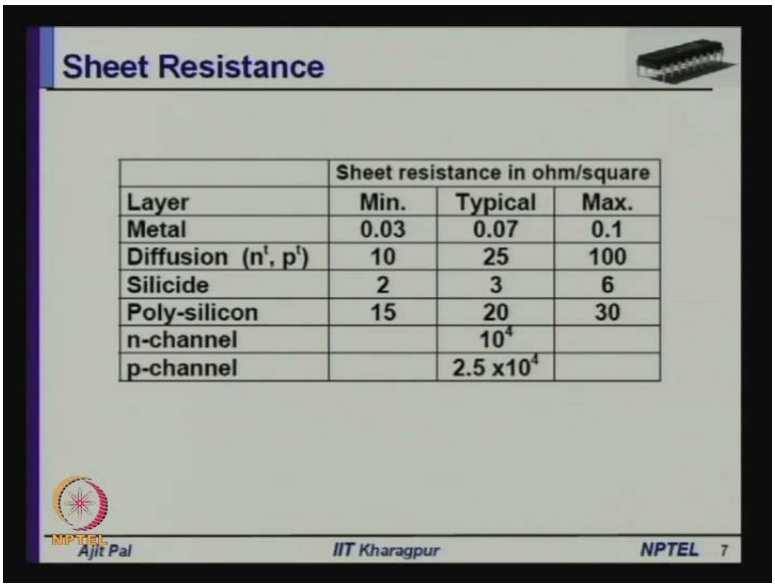

So, in terms of this seat resistance we can calculate the resistance of a conducting material and these are the typical values of seat resistance for different conducting material which are used for the realization of MOS transistors. We know that we shall be using metal for taking interconnection we can see the seat resistance that is per square is I mean; obviously, for metal it will be very small where it is a very good conductor metal essentially is aluminum and typical value is 0.07 and; obviously, it will have some minimum and maximum value because the thickness resistivity of aluminum is fixed, but thickness will vary whenever you do the fabrication. So, it will vary from fabrication technology to fabrication technology as a consequence the seat resistance will vary and for a particular fabrication technology this is given similarly, for diffusion layers for n type as well as for p type the seat resistance is typically 25 per square minimum is 10 per square and maximum is 100 per square again, that thickness of diffusion that you know that depth of penetration of the diffusion layer.

Will vary from fabrication technology to fabrication technology that will lead to different seat resistance for the diffusion layer similarly, silicide that is also used in the implementation fabrication and you can see it has got some resistance not very high resistance 3 ohms typically, but poly silicon as you can see which is used for you know interconnection over short distances. So, poly silicon is used as interconnecting material for connecting say from drain to gate of front transistor from drain of front gate transistor to gate of another transistor and so on, for short distances and there resistances are the

seat resistances are linear on the other hand the n channel and p channel you know that resistance is quiet high.

That typical value of resistance of n channel is 10 to the power 4 power square for n channel and for p channel; you know it is still more because of lower mobility of force that is 2.5 into 10 to the power 4 ohm's per square. So, you see these are the typical value of seat resistances of different types of conducting materials.

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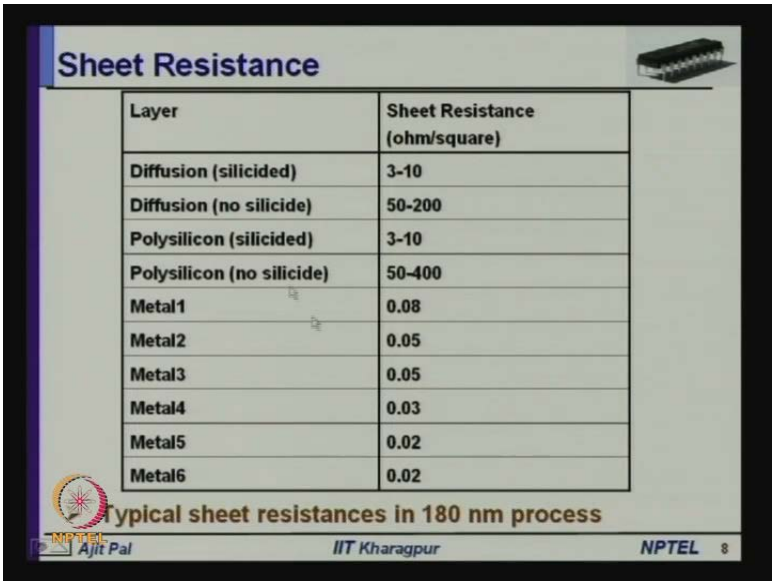

And in fact, here for a particular process of technology 180 nanometer process technology that previous one was for little higher process technology may be 5 micron or so, and this one is for 180 nanometer. So, it is still old, but you can see the values are little different. So, for the diffusion layers you can have 2 types of diffusion layers one is silicided and other is no silicide. So, in that case you can see the seat resistance will vary from 3 to 10 ohms without silicide silicide and no silicide then 50 to 200 ohms for poly silicon when it is silicided it is 3 2 ohm's again and for poly-silicon.

So, you can see diffusion in poly silicon when silicided they are giving more or less the same resistance shows the diffusion layer and poly silicon layer are also providing more or less similar kind of resistances. However, the different types of metal layers are used in a present day VLSI technology a number of layers of material is used and as a consequence there is thickness and there and the value of t is different as a consequence we find there that there seat resistance is varying from 0.08 to 0.02 metal 1 metal 2 metal

3 metal 4 metal 5 metal 6. So, these are the typical seat resistances in 180 nanometer process and this these information can be used for the calculation of delay later on we shall discuss about it.

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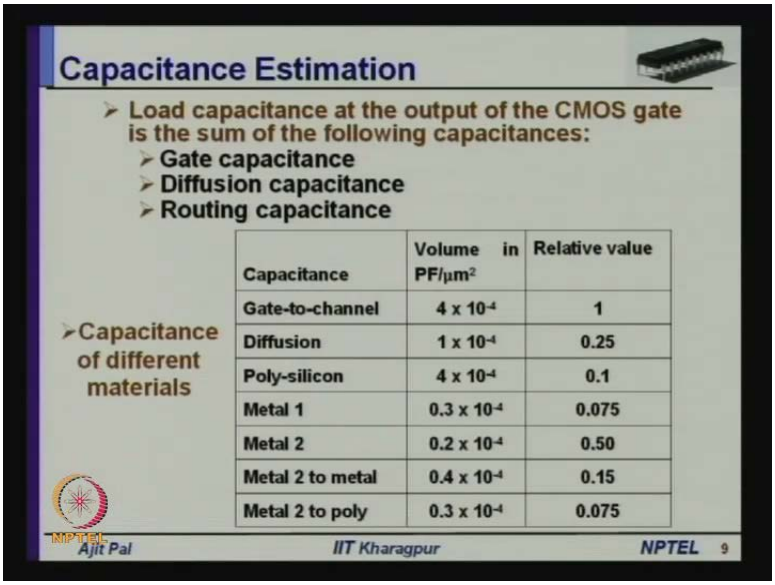

Coming to another very important parameter that is your capacitance estimation we find that load capacitance at the output of a CMOS gate is a sum of the following capacitances you know, if you consider a CMOS inverter then at the output you will face these three capacitances gate capacitance gate capacitance is essentially I believe, I have a diagram.

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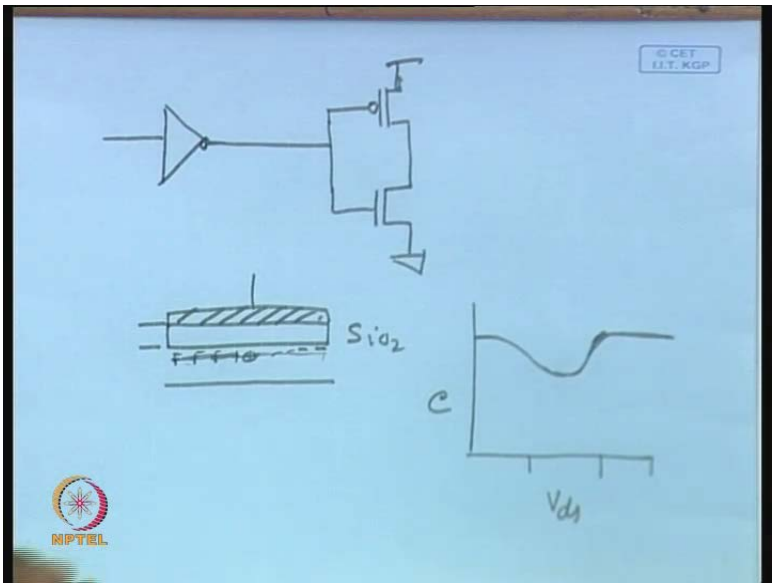

I shall let me draw a diagram say this is an inverter this will be connected to may be another stage of inverter or some more complex circuit. So, you see here it will face the gate capacitance of the next stage. So, gate capacitance of the next stage that is what is being shown here gate capacitance of the next stage then diffusion capacitance. So, diffusion capacitance is essentially the capacitance for this particular stage, we shall show it in more detail in subsequent slides then routing capacitance, because you have to take interconnection from output to the input of the next stage and this interconnections will have some capacitances.

So, you can see the capacitances for different materials is shown here gate to channel that is that will actually the characterize the gate capacitance 4 into 10 to the power minus 4 picofarad micron square considering this as the standard and everything is normalized with respect to this then the diffusion layer has got one fourth the capacitance compared to gate channel so; that means,. So, gate channel gate to channel has the maximum capacitance compared to other regions.

So, diffusion layer has one fourth the capacitance picofarad per micron square poly silicon has 0.1 0.11 tenth of that of the gate capacitance metal has still over capacitance 0.3 into power 10 to power minus 4 picofarad per micron square metal 2.2 into power minus 4 picofarad per micron square then metal 2 to metal layer whenever the VSLI fabrication is done in a multiple layers nowadays the VLSI fabrication is done in

multiple layers. So, there will be one metal layer and below there can be another metal layer.

So, that will also lead to some capacitance metal 2 to metal point 4 to 10 to power minus 4 capacitances. So, you see the capacitance is a little high compared to that poly silicon then metal 2 to metal 2 to poly 0074 here it is very small. So, you find these are the different types of capacitances that you will encounter whenever you realize a circuit VLSI circuit and coming to the gate capacitance we find that MOS capacitor depends MOS capacitance we have seen typical value is 4 into 10 to power minus 4.

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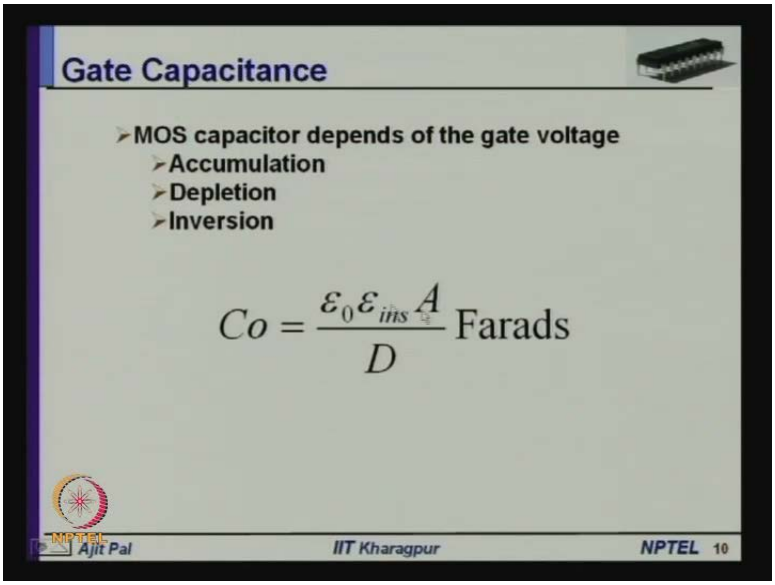

But actually it is not fixed. Dynamically the gate capacitance will change depending on in which mode it is we have already seen the MOS transistors will be in accumulation stage initially when the gate voltage is small less than the threshold voltage. So, in that case you know that channel region will be filled up with the carriers of the original device; that means, sub state for example.

Whenever, if you are using p type sub straight holes will be there. So, presence of holes will be there and as a consequence in the accumulation mode capacitance will be quiet high because capacitance will dependent on suppose this is your silicon dioxide and here, it is poly silicon, I am drawing a channel region, then this is the sub straight. So, this is the sub straight and this is the sub straight and initially as you have seen there will be holes present here.

So, the thickness of the conductor will be the thickness of the silicon dioxide. So, the if we plot the capacitance as it moves from accumulation to depletion to you know that inversion as we increase the V D S then the capacitance will change and particularly when it reaches the depletion region this part will be divide up in a charge carrier there will be no charge carrier. So, it will be depleted. So, effectively that will increase the thickness of this silicon I mean the insulators.

So, as a consequence in the in the in the depletion region the capacitance is less, but again when inversion layer is created there will be electrons here. So, again thickness will reduce and capacitance will be more. So, what I am trying to say here the capacitance value of the gate region is not fixed. It depends on the gate Voltage that you are applying and because of the different values of the voltages the device moves from one mode to another mode accumulation to depletion to inversion mode and accordingly the gate capacitance will change.

And gate capacitance can be estimated as epsilon 0 that is the permittivity of the v space and epsilon I N S insulator that is silicon dioxide typical value of this is 3.9 as we have seen and A is the area of the that length into width, and these are thickness of the silicon dioxide. So, this is typical value of gate capacitance, but again we shall see that particularly this thickness will change and that will lead to different values of the gate capacitance as it goes from one mode to another.

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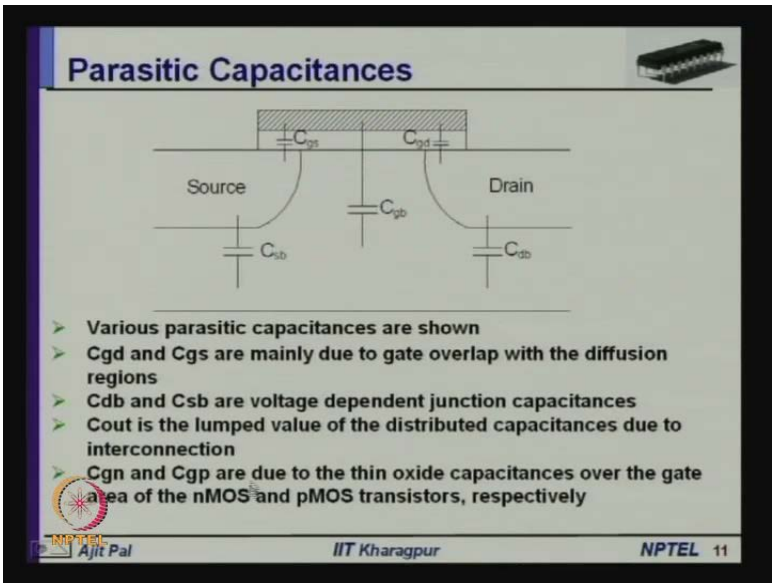

Coming to various Parasitic Capacitances we find that different types of parasitic capacitances for example, Cgd and Cgs. So, here you have got Cgd here gate to drain and gate to source. These Cgd and Cgs are essentially because of overlapping of the gate reason on the source and drain reasons on the diffusion reasons and as a consequence this will have some capacitance Cgs and Cgd due to the gate overlap with the diffusion regions. Similarly, C db here you have got C db drain to body and source to body these capacitance because this part will be there will be depletion region there will be depletion region here, as well this will probably lead to some capacitance as you know this is n class and this is p.

So, there is a diode and this they it will have some capacitance that is your C db and C s b. So, these 2 are Voltage dependent junction capacitances, because they are as we have seen they are reverse bias diodes and depending on the reverse bias Voltage there capacitances will vary and as a consequence they are Voltage dependent junction capacitances and C out is another capacitance that will encounter whenever you interconnect a inverter to other parts of the circuits that is essentially, the distributed capacities due to interconnection.

C out is not shown here as I shall see in the next diagram. Similarly, Cgn and Cgp are due to the thin oxidation capacitances over the gate area. So, here and the gate area this is you C g b Cgn and C g b actually, C g b is a generalized form of capacitance in case of n type nMOS transistor this will be C g p, because this body this sub state will be p type and for p type transistor and this will C g n, because it will be n type sub state. So, Cgn and n Cgp are due to thin oxide capacitance over the gate area of the nMOS and pMOS transistor respectively.

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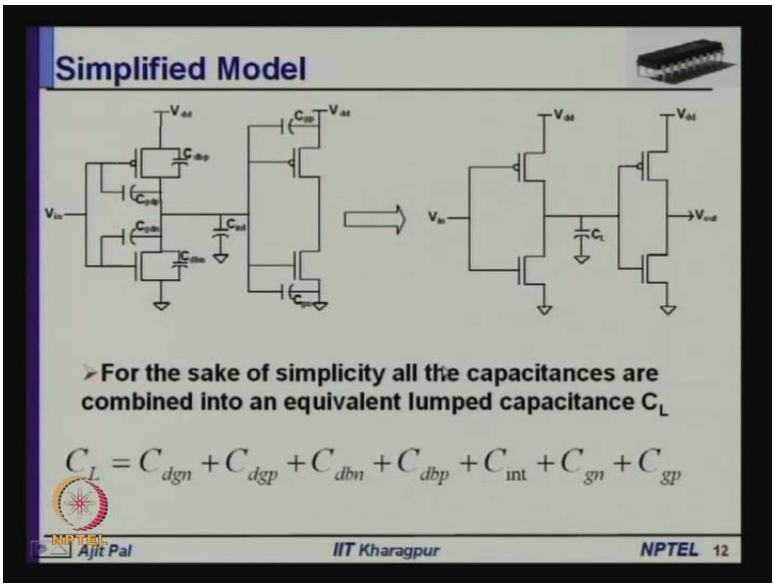

So, these are the various capacitances you will encounter, and this is the simplified model that we can make from this. So, here what we have shown this is an inverter, with it are associated capacitances is, so this C interconnect is that interconnect capacitances that I mentioned, and here are the Cgp and Cgn it is encountering the diffusion, these capacitance it will encounter this output will encounter, what we can do? We can see that the effective load capacitance C L is essentially, sum total of C dgn and C dgp, C dbn, C dbp, C interconnect Cgn and Cgp, because we have so many capacitances associated with it, and these capacitances can be lump together for the sake of simplicity to had to define a single capacitance C L load capacitance. So, later on we shall be referring to a single capacitance that is C L load capacitance, but essentially it comprises many capacitances gate capacitance, then to body capacitances interconnect capacitances and. so on which I have shown in this diagram.

So, let us assume this is our simplified model for estimating the delay characteristics of an inverter. So, one inverter is driving another inverter with a load capacitance C L. So, this is our simplified model.

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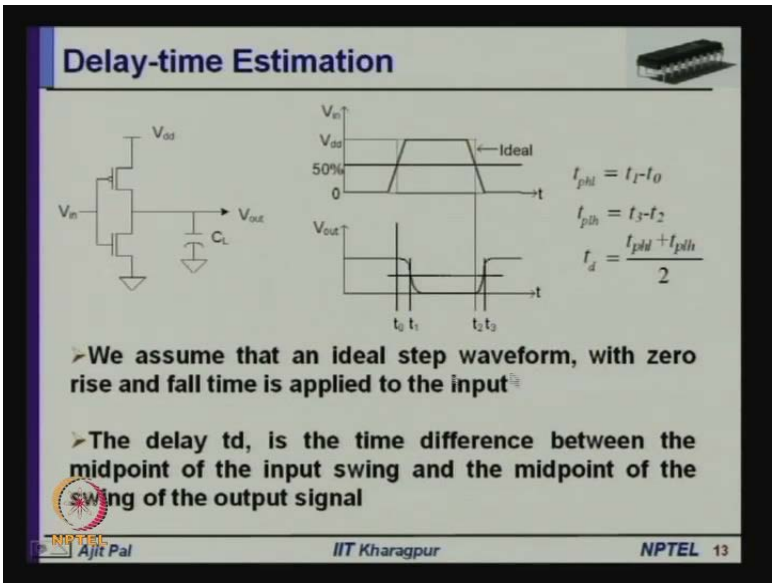

So, how do you define delay of a gate? So, here we have removed the other gate because we have the representative load capacitance C L which has taken into consideration we gate capacitances. So, how do you define delay of a gate? So, here we have removed the other gate, because we have the representative load capacitance C L, which has taken into consideration the gate capacitances of the next stage.

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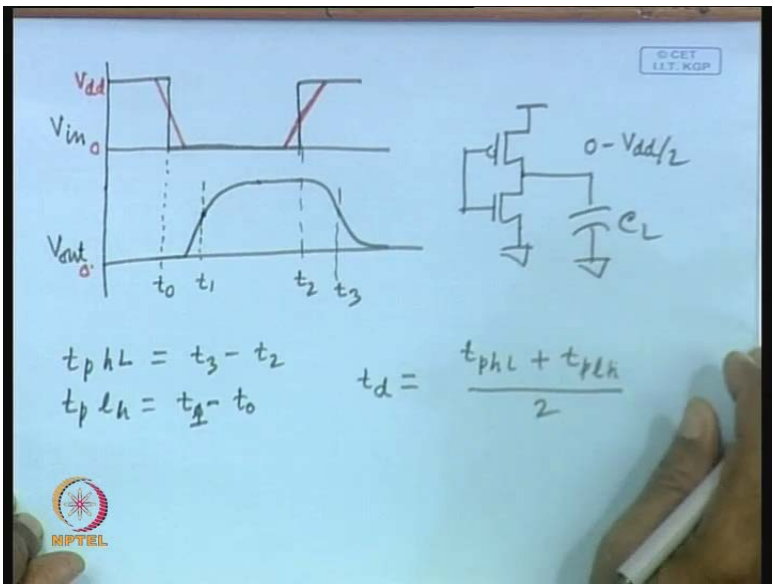

So, how do you define delay? You see normally what you apply an input V in and it produces a output a device.

Now, that input you know we can assume that the input is changing quickly, here also it is changing quickly; that means, step input; that means, the switching times rise time and fall time of the input is 0, but ideally this will not be so; that means, later on you will see this will be there will be some finite it will take some finite time change from 0 to V dd to this is your V dd and this is 0 Volt and this is the 0 level of the output and as the input of an inverter is changing from V dd to 0 output will change from 0 to V dd and; obviously, this output will change after the delay time.

So, here you can say this is where the input has changed. We can consider the middle point of the output I mean an input as the reference with reference to that, it will it is changing from V dd to 0 here it will change from 0 to V dd. It will not we have seen the characteristics it will change the capacitor has to charge. So, it will have a nature like this. So, we can take the middle point as the to define the delay time. So, delay time for; that means t t p high to low and t p low to high we can draw. So, t p high to low this is essentially, the t p low to high. So, t p low to high is this is you t 0 and this is your t 1. So, this is t p low to high we can draw. So, t p high to low this is this is essentially the t p low to high this is t 0 t 1 minus t 0. Similarly, here the output we may say that here also it does not change quickly.

So, let us assume this is the this is the nature of the input and as a consequence here also it will change like this, and we can consider the middle point and this is this point as a reference this is your t 2 and this is you t 3. So, this is equal to high to low time is you t t3 minus t 2. So, this is the typical time for transition from high to low, this is the transition from low to high. So, these are the 2 times, we can measure, and then the later on we shall see that this low to high and high to low times are not same. We have already seen there is some asymmetric behavior of the inverters the pull up transistor resistance can be different from a pull up pull down transistor resistance.

Unless we explicitly the design the circuit if they are if the same dimension there resistance should be different, that will lead to different rise time and fall time as a consequence what we do we measure we take the average that is you t d t d is equal to t p high to low plus t p low to high by 2 that is defined as the delay time. So, this average value is considered to be delay time of the device, question is how do you really measure this delay time? And to measure the delay time, we can have a very simplified model what is that model for an inverter say whenever we are.

Let us consider this case, when it is charging from I mean, it is going from input is going from low to high; that means, we have your there is a pull up device is on which is responsible for the change from 0 to high low to high.

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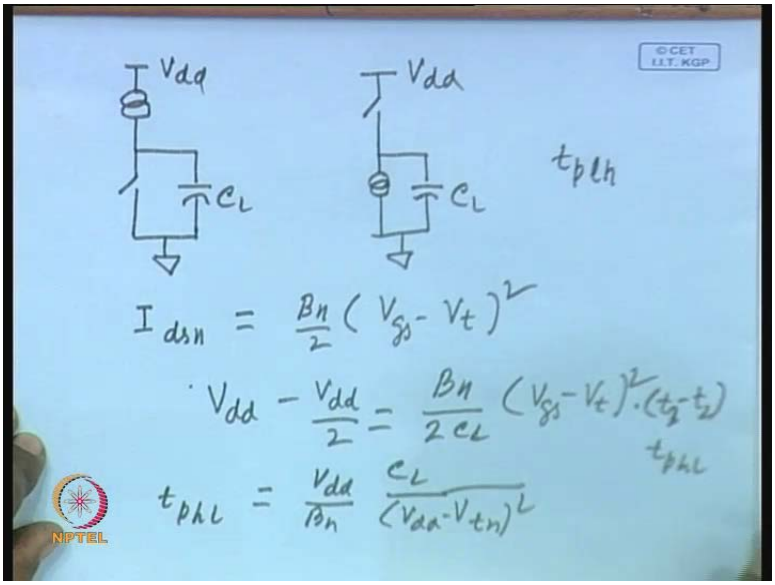

So, in that case what we can do we can moderate this way. As if a this is your V dd and this is your load capacitance C L and here there is a switch and in this particular case whenever it is switching from low to high, this capacitor is charging from low to high then this switch is off, this is representing the pull down device, and this is representing the pull up device. You may be asking why you have represented this device as pull up device, the reason for that is in this particular case as you can see during the period it is changing from low to high output is essentially, that input to the you know that this particular device.

Let me draw it an inverter that will make it clear. So, hear you have got a capacitance connected to ground C L. Now it is charging through this part it is charging now it is charging from 0 to V dd. So, what is the state of this device that time what input you have applied to it, when it is output when the input is V dd. So, input is V dd is applied here and it has switched to zero; that means, most of the time you can see the input is varying from 0 to V dd and this output is changing from 0 to V dd; that means, the Voltage across this device is varying from 0 to V dd by 2. So, since it is varying from V dd by 2, you may assume that this transistor is in saturation and as you know.

When a transistor is in saturation, the current remains constant and that is the reason why the pull up device has been approximated as a constant current source in this particular case. So, when it is charging it is assumed to be a constant current source which is responsible for charging the device. Similarly, you know whenever we are discharging it we shall consider this that the pull up transistor is off and we have a constant current source which is discharging this capacitor C L, C L is getting discharged through this path and through this constant current source.

So, and we shall assume that both the transistor are in saturation when this charging and discharging is taking place. So, this is V dd and this is ground and as a consequence, we can write down the expression for current d s n in this particular case will be equal to beta n by 2 into V g s minus V t square we know that. So, this is charging from 0 to V d t and; obviously, the since it is discharging through a linear current path it is discharging from 0 to V dd to in this case V dd to V dd by 2 initially it was V dd then V dd by 2. So, in this case we can say that time will be equal to V dd minus V dd by 2 will be equal to beta n by 2 C L into V g s minus V t square into t 1, I mean that time that we have shown this whenever it is this particular high to low, so t 2 minus t 3 minus t 2. So, this is your t p high to low. So, this if we substitute here.

We shall this is V dd by 2 this 2 will cancel out and we shall be having an expression for t p high to low that is equal to V dd by beta n this will got to add the denominator into C L by this will go up C L by V dd minus V t n square. So, this is the expression that you will get. So, this is the expression for t p high to low. Similarly, we can find out the value for the other one t p low to high what is the difference between these 2, difference is in case of pMOS transistor it is nMOS transistor otherwise it is different it is same.

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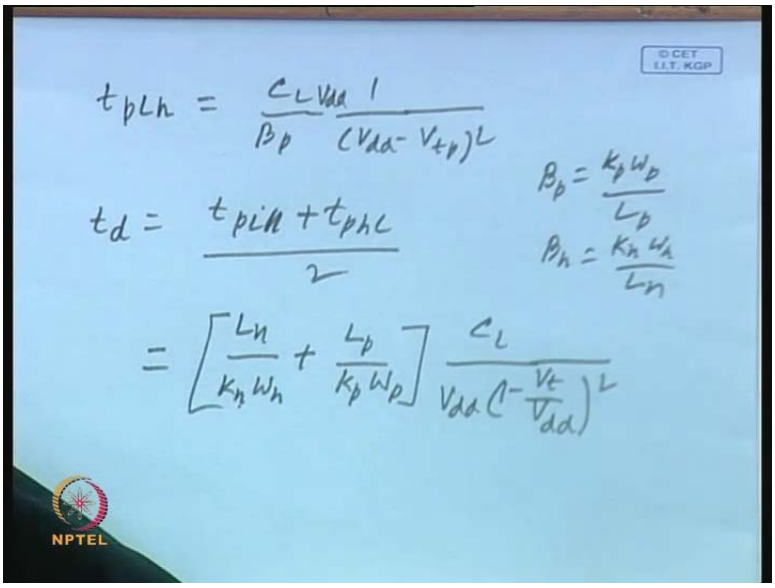

So, we can write the own expression for t p low to high is equal to C L by beta p beta is K W beta p is equal to K p W p by L p into one by same here you can write V dd V dd minus V t p square. So, this is the expression that we can write. Now what is the delay time t d is equal to t p low to high plus d p high to low by 2. So, this will be equal to by substituting beta p in place of beta p is equal to K p W p by L p as we know and similarly, for beta n is equal to K n W n by L n.

What the expression we shall get will be equal to L n by K n W n plus L p by K p and W p into C L by V dd into 1 minus V t by V dd square. This is the expression that we getting ultimately for the delay time you may be asking how we have got this figure actually V dd was at the eat the numerator what we have done we have taken out the V dd outside. So, it has become V dd minus V t p or V dd minus V d n and one V dd has cancelled out and here we are getting V dd minus V t p. So, what does this expression tells us? This tells us various about various parameters on which the delay will depend; obviously, delay will be more if the length of the devices is more; that means, the it will take longer time for the electrons to move from one end to the other end. Similarly, if the width is more then also delay will be delay will be less and there is a parameter we here, mobility of electrons and hole that part will also be K p and K n has got.

Those parameters mobility of electrons and mobility of holes they will also be responsible to define the delay, but one those are fixed parameters on which I mean of

course, length and width we can change we cannot change K n or K p, but what kind of dependence it has got on C L.

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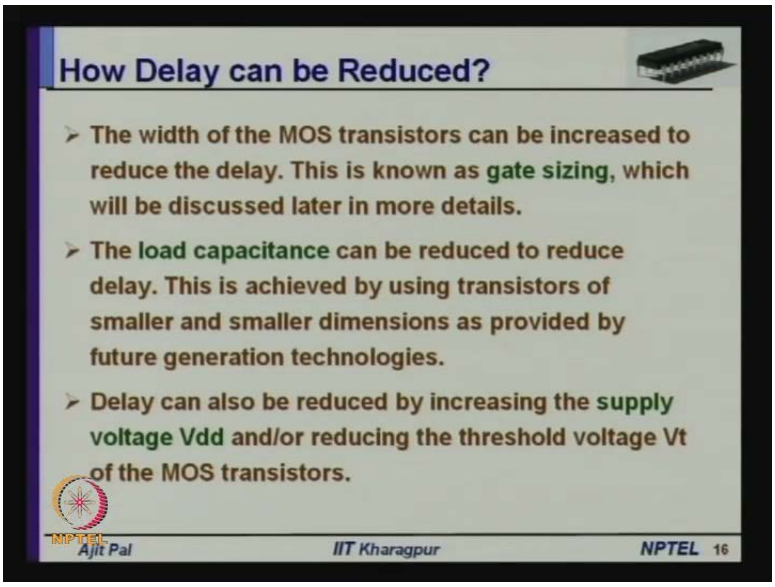

Actually, we can say we can discuss in more detail here say how delay can be reduced on what parameters it has got dependence. So, the width of the MOS transistors can be increase to reduce the delay and this is this particular technique is known as gate sizing, later on we shall discuss about it in more details. Then load capacitance, we have seen there is parameter called load capacitance on which there is strong dependence as a consequence the load capacitance can be reduced to reduce delay and you know, how it has been done as we go from one technology generation to the next technology generation the dimension of the device is reduced. That effectively reduces the capacitances and actually Mohr's law has flourished based on this; that means, capacitances have reduced the performance has increased delay has reduced the devices can operate at higher and higher frequency.

So, and last factor is delay can also be increased by increasing supply Voltage V dd we have seen in this expression V dd is present here. So, by increasing V dd the delay can be reduced, but unfortunately as you increase the supply Voltage the power dissipation increases, because power dissipation is proportional to V dd square that is the reason why normally we do not want to use the increase the supply Voltage rather the supply

Voltage has to be reduced, but we have to see how the performance can be maintained even when the supply Voltage is reduced that is the challenge of low power design.

Now coming to this part of the expression this is very interesting we can see here this is one minus V t by V dd square it is in the denominator. Now if as you reduce V dd whenever you go from one technology generation to next technology generation you can also reduce V t in the same ratio an as a consequence the V t by V dd ratio is maintained to maintain the same performance, but if you do not do that, if you simply reduce the supply Voltage without resuming the reducing the threshold Voltage what can happen you will see this value will keep on reducing I mean, V dd is reduced. So, this value is increasing will be increasing and whenever V t will become very close to V dd that time this will be very close to one.

So, when the denominator is this particular part is very close to one, this will have a very small value and the square of that will have still smaller value and then the delay will be very large; that means, when the supply Voltage is close to the threshold Voltage delay increases dramatically. So, that is the reason why we should not use supply Voltage close to the threshold Voltage normally typical value of V t is in the range of 0.2 V dd to 0.5 V dd . We can see this is the safe operating range; that means, we can get reasonable performance whenever the threshold Voltage is kept in that range. So, that is the reason why in my last lecture I was mentioning that the C-MOS inverter will keep on functioning even when the supply Voltage is equal to threshold Voltage or less than threshold Voltage the delay will be very large.

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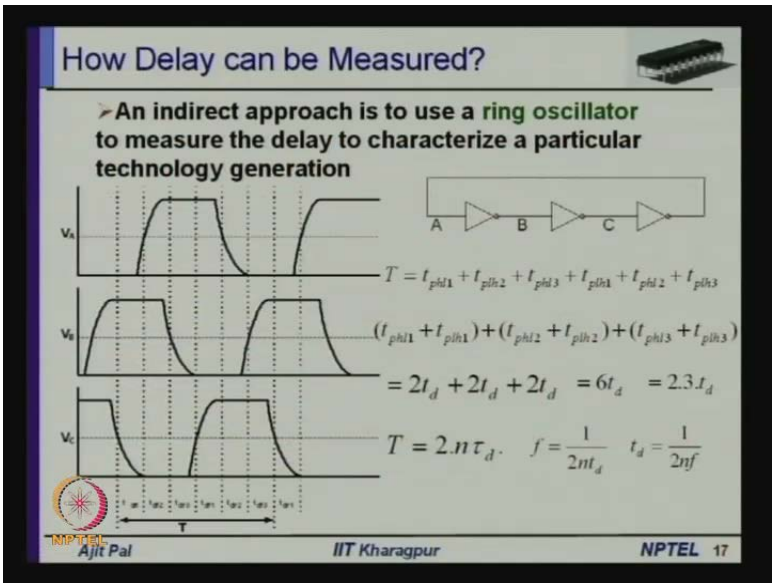

Now another question arises how delay can be measured? How Delay can be measured? So, delay value is very small it is in the for present day technology it is fraction of nano second you know the devices are the operating rough frequency few Gigahertz and the consequence the delay will be few I mean, nanosecond or fraction of nano second how do you measure it we cannot measure it with the help of oscillator. So, a special type of circuit is made known as ring oscillator, and ring oscillator is fabricated using the devices of the of the generation inverters of that generation and then the delay is estimated how let us see. Question is, what is a ring oscillator?

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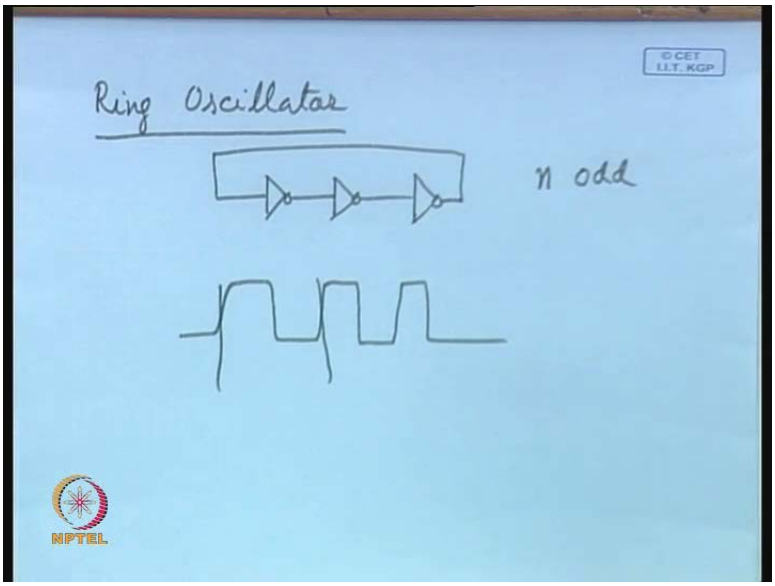

A ring oscillator can be realized with the help of several inverters in this form what you will do to realize a ring oscillator, we shall use odd number of inverters 3, 5 say 3 and then we shall apply this output to this input. So that means, 3 inverters connected back to back and this will form a ring oscillator; that means, value of n number of inverters present has to be odd then it will form a oscillator.

What is the function of a oscillator it will generate, it will oscillate and generate clock, then the time period of the clock can be measured question is on what factors the time period depends. Let us see from this diagram as you can say here, I have plotted the voltage of three different points this is this is three inverters connected to realize a ring oscillator point A point B point C. So, point A is the input of the first invert point B is the input of the second inverter point C is the input of the third inverter.

So, here assuming that it will oscillate, so here say this is the delay time this one between one line and another line this is the delay time. So, when at this point it is changing from 0 to V dd next stage will change from V dd to 0 after we get the delay time next stage here. So, here it will delay; that means, after the delay time it will switch from high to low. So, here it has change from low to high here it has change from low high to low.

Similarly, this will lead to a transition of this inverter from low to high. So, B at point C at output C at point C we will have a transition from low to high after delay time. So, in this way and again this C is now this output of C it is essentially point A. So, point a will switch now from high to low, because it has change from low to high this output will this output of this inverter will change from high to low. So, in this way we can see I have plotted several wave forms and we can see this is the time period that will be true for at point a point b or point C at all the point.

So, this total time, this is a time period of the clock that has been generated with the help of this ring oscillator and this particular time period is equal to the rise time and fall time t p initial 1 that is the first stage t p low to high of stage 2 t p high to low of stage 3, then again t p low to high of stage one and so on. So, this total time comprises these delay these time and they can be clubbed to t p is t p t p is l 1 and t p h l 2 these two can be confined and this is equal to 2 d. As we know d p h l 1 and t p l h 1 by 2 is equal to t d this is equal to t d this is another t d. So, we have got 6 t d. So, 6 t d is equal to 2 into 3 t d and since n is the number of stages here this is 2 into 3 into t d. So, we can say that the

time period is equal to 2 and n is the number of stages of the inverters into tau d that is the delay time of a particular stage. Now instead of t, we can express in terms of frequency of oscillation as well. So, f is equal to 1 by 2 and t d. So, what this?

Whenever we want to measure this delay, what we can do? We can extend the time increase the time period by increasing the value of n typically, we can have say as large as 101 inverters or 151 inverters and using that we shall form a ring oscillators not 3 or 5. So, when you have got large number of inverters and they are connected that we have the delay time will be easily measurable with the help of the equipment the we that we that is available at our disposal. So, to measure the delay time, we use the ring oscillator having large number of stages may be 101 or 151 or so; that is how whenever a new generation technology is introduced, its delay time is measured to characterize the new generation technology. So, you have seen, how delay can be measured.

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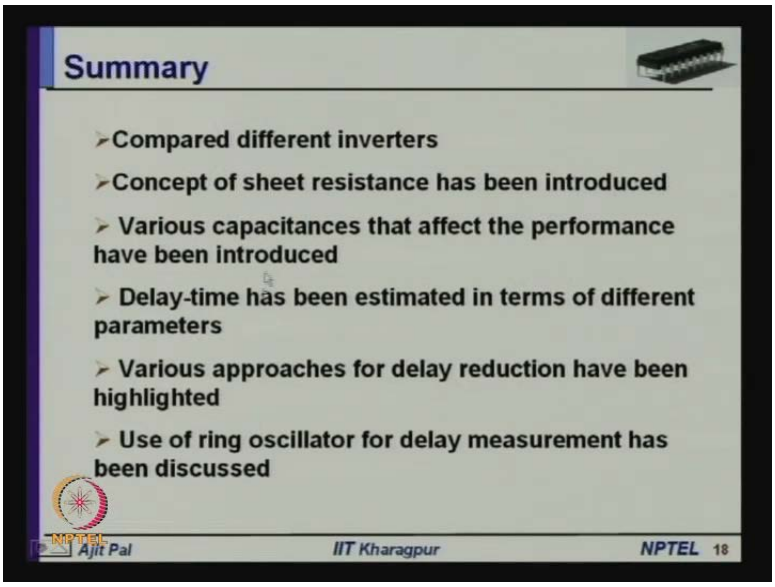

Now it is time to summarize what we have discussed. We have compared different types of inverters, the performance of different inverters, and we have seen C-MOS in the inverter of choice; we have introduced the concept of seat resistance, we have introduced various types of capacitances that you encounter in a VLSI circuit, and we have discussed how delay time can be estimated, and I have highlighted how the delay time can be reduced by controlling different parameters finally, I have discussed the use of ring oscillator for delay measurement. So, with this we have come to the end of today's

lecture; in the next lecture, we shall discuss how large capacitances can be driven by inverters, thank you.