Low Power VLSI Circuits and Systems

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Lecture No. # 07

MOS Inverters – II

Hello and welcome to today's lecture on MOS inverters. This is the second lecture on this topic. In this lecture primarily I shall discuss about c MOS inverter. However, I shall discuss about some other things as well.

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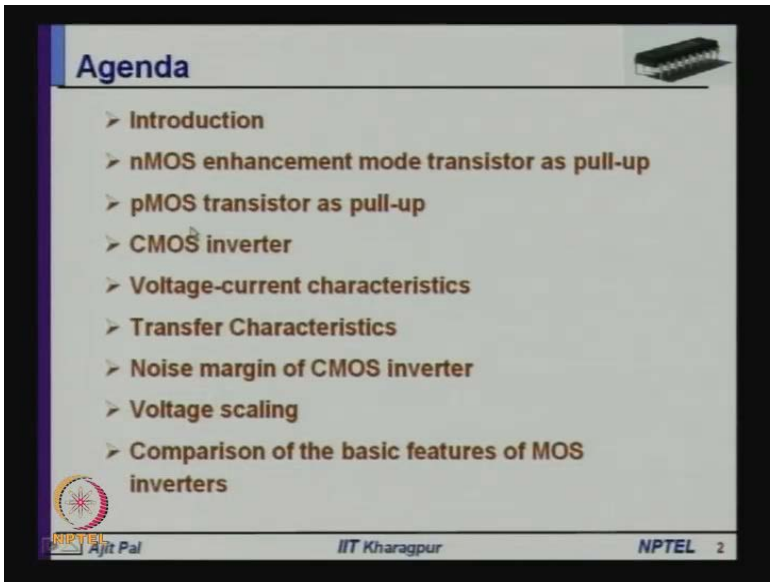

So, here is the agenda of today's lecture. After giving a brief introduction where I shall discuss what we have covered in the last lecture; I shall discuss about n MOS enhancement mode transistor as pull-up device and then realization of inverter using p MOS transistor as pull-up device.

Then as I told, I shall cover in detail about c MOS inverter. Then various characteristics of c MOS inverter like voltage current characteristics, transfer characteristics, noise margin and voltage scaling as you reduce the voltage how it behaves. Then I shall conclude my lecture by comparing the basic features of different types of MOS inverters.

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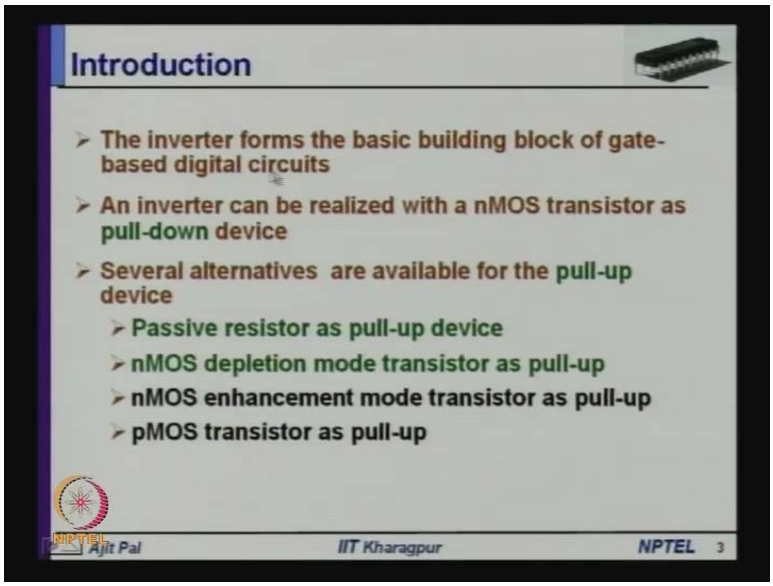

As I mentioned in my last lecture; the inverter forms the basic building block of gate-based digital circuits and as I have shown an inverter can be realized with a n MOS transistor as a pull-down device. And of course, you we have got several alternatives for pull-up device starting with passive passive resistor n MOS depletion mode transistor which we have covered in the last lecture and today we shall be discussing about n MOS enhancement mode transistor as pull-up and followed by p MOS transistor as pull-up.

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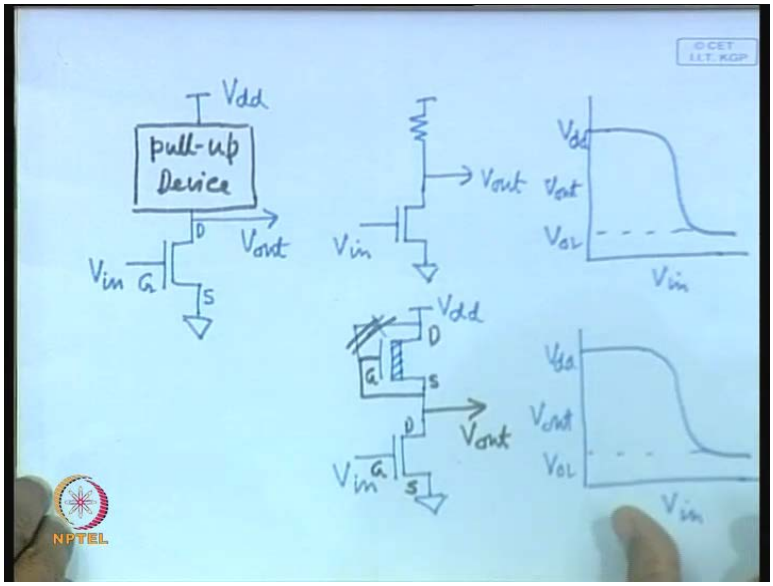

So, as we have seen an inverter can be realized very quickly. Let us recapitulate what we have discussed in the last lecture. We require a pull-up device.

Pull-up device and the pull-down device, is the is a n MOS transistor which is connected to ground the source is connected to ground, this is the source and this is the gate and this is the drain of this n MOS transistor and input is applied to to the gate of the n MOS transistor and the pull-up device is connected to V d d. And output is taken from here. This is your V output and we have discussed two alternatives in my last lecture. First one was to use passive resistor as the pull-up device and we know that in that case we shall be using a passive resistor as pull-up device then n MOS transistor as pull-down device and output is taken as usual from here, V out and V in is applied here and we have discussed the various limitations and characteristics of this type of inverter.

And particularly we have discussed the transfer characteristics where we have seen it it gives a strong output. I mean high level output V d d but, low level output is not 0. So, there is a, the volt is above 0 volt. So, this is the input output characteristics V out and V in and and we have discussed various limitations of this type of inverter. We have also considered the realization of n MOS depletion type device as the pull-up device. This is the representation of a depletion type n MOS transistor and then a n MOS enhancement type transistor is used as pull-down device. Input is applied here and this, since this is always on when gate is connected to source. So, we connect it to this point here it is your here is your V d d.

Sorry sorry I have made a mistake here. It will not be connected here actually it will be connected to source not to the drain but, to the source. So, not to this one. So, this is always on when it is connected to this source and this is the drain and this is the gate of this transistor and this is the gate source and drain of this transistor and output is taken as usual from here V output and in this particular case also you have seen that the the transfer characteristic is somewhat similar to the the realization by using resistor as the pull-up device, passive resistor as pull-up device. So, here also the characteristic is somewhat transfer characteristic is somewhat similar.

We get V in, I mean V, V in V out there is a transfer characteristic we get strong output high level output, but, the low level output is not 0. But, it has some other features like it is a ratioed logic because you have to maintain a ratio between the length of the length

by width of the device of the pull-up device and the length by width of the pull-down device. That is why it is called ratio ed logic and we have seen there is a static power dissipation in both the cases. Now, let us focus on the use of depletion mode n MOS enhance mode transistor as pull-up device.

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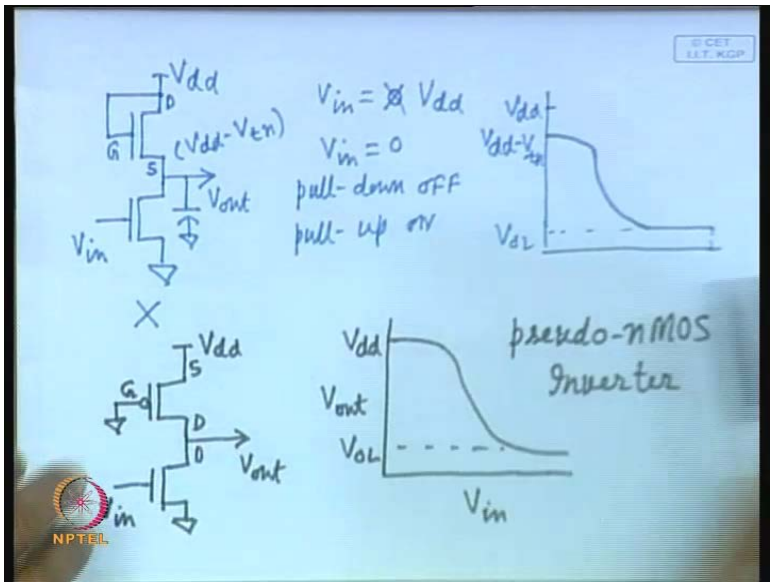

The third type which we did not discuss in the last lecture. That means, we have a n MOS enhancement type transistor as pull-up device and then n MOS enhancement type as pull-down device.

Here, this has to be connected to V d d. So, that it transform. So, in since this is a enhancement type transistor you have to apply some gate voltage which is of, which have to be above the threshold voltage. So, that it transforms and you will get an output which is I mean. So, that this transistor is turn on is on and you will take the output from here. So, this is your V out and now in this particular case what will be the transfer characteristic? Let us have a look at the transfer characteristic of the device without discussing about the input output characteristic. Here, as you can see the output whenever the input is 0; output is supposed to be V d d for a for an ideal inverter, but, as you can see we are not getting output which is equal to V d d. But, you are getting V d d minus V t n where V t n is the threshold voltage of the n MOS transistor. Why so?

The reason for that is let us consider that there is a capacitor here as you know in a, in a in case of an inverter there will be output load capacitance. So, a capacitance is

connected to the output and as a consequence suppose the output is changing from 0 to V d d. So, when what is the initial condition when V in is equal to 0? Let us assume initially it was not v in is equal to 0, but, it was V d d. Then as we know this transistor, this output will be output will not be equal to V d d. But, it will be little less than V d d because this transistor is on, this transistor is also on and as a as a consequence you will get a output which is not really 0, but, V o l. So, V o l when input voltage is V d d. So, here you will get V o l.

Now, as the input switches from V d d to 0 then what happens? So, then what happens this capacitor will charge from V o l and it will charge towards V d d because this transistor is on and this transistor is now off. So, your pull-down is off in this particular condition. Pull down transistor is off and pull-up is on. Let us not bother about at this moment. What are the, in which state they are in, whether they are in saturation mode or linear mode let us forget about that for the time being. Now, this transistor is off and this transistor is on as a result this capacitor will charge and output voltage V out will gradually rise from from V o l towards V d d.

What a point will reach when this voltage which is supposed to be source, this is the drain and this is the gate. When this voltage you see here we have applied V d d and when this voltage reaches V d d minus V t n where V t n is a threshold voltage of this transistor; then what will happen? Then this transistor will turn off and as a consequence the output will not charge beyond V d d minus V t n. So, here as you can see we are getting a high level output which is not really V d d, but, we are getting less than V d d. As a consequence we find that in case of an inverter where we are using n MOS enhancement mode transistor as pull-up device; neither the high level output is strong nor the low level output is strong. Both are weak; that means, in case of 0 output we are getting V o l which is above 0. Similarly, for high level output you are not getting V d d, but, which is less than V d d V d d minus V t n.

So, these these are the characteristics and as a consequence we find that we are this particular type of inverter is not really very good good in a sense that since both are weak this is not really suggested. I mean not recommended for use in real real life circuits. So, here we find that output is not ratio less. That means it is also ratioed logic because when the input voltage is V d d we have seen that output will be dependent on the, of this transistor and the on resistance of this transistor; that means, they they will act as a

voltage divider and output will be as we have seen it is v o l. So, it is also not raioless in other word it is also ratioed logic.

And as we know whenever it is ratioed logic; the the pull-up resistor has to be at least four times higher than the pull-down resistor. So, in such a case we never get symmetrical switching characteristic. So, that is another limitation of this inverter. So, you do not get symmetric switching characteristic and there is static power dissipation when the output level is low. As you have seen when the input is 0, both the transistors are on. So, current will flow from V d d to ground. As a result there will be static power dissipation in this circuit and you will not get, I mean the power dissipation will be high.

And I have already mentioned about this. It produces weak high output and level and weak low output level because of all these things as I have already told this particular inverter is not really, not recommended. So, this is never used. Now, let us switch to another type of inverter where we can use p MOS transistor as pull-up device. p MOS transistor as pull-up device when it is used then as you can see the p MOS transistor is is this is connected to ground. That means, it is always on because let me draw it and explain once again.

So, here we have got p MOS transistor of course, p MOS enhancement type transistor as pull-up device and a n MOS depletion type transistor as pull-down device as usual. So, you are applying input voltage here. This is connected to ground and we can consider this as source, this as gate and this as drain in case of a p MOS transistor. Since this is connected to ground and the voltage is always minus V d d; that gate voltage with respect to source is minus V d d. So, this transistor will be always on and as you can see this drain of the p MOS transistor and drain of the n MOS transistor are tied together and here you get output V out.

So, in this particular case what will be the transfer characteristics? So, when the input voltage is 0; I mean when the input voltage is 0 this transistor is off, this transistor is on. So, we and s through this you will get a output since this transistor is always on as I have told because you have maintained a gate voltage of V d d minus V d d between this gate and source and this transistor will be always on. So, the transfer characteristic will be somewhat like this you will get a strong high level output V d d when input voltage is 0

since this is off and this is on. But, as you increase the voltage and when it the the input is V d d then the characteristic will be somewhat like this.

That means you will get the voltage. Again a low level voltage which is not 0, but, little above ground voltage ground level. So, this is the transfer characteristic of this inverter where a p MOS transistor is connected to the connected to the I mean as used as pull-up device. Now, you may be wondering why this particular inverter is called pseudo-n MOS inverter? This is not a, I mean you are using a p MOS device as the pull-up device. The reason for that is you will find there is close similarity between the transfer characteristics of this inverter where you have used a n MOS depletion type transistor and where you have used a p MOS transistor as pull-up device. We see the transfer characteristics is almost same.

So, it is identical and since they are identical their characteristics are same. They are instead of calling them p MOS, I mean p MOS inverter it is called pseudo-n MOS inverter pseudo-n MOS inverter and what are the typical characteristics of this inverter?

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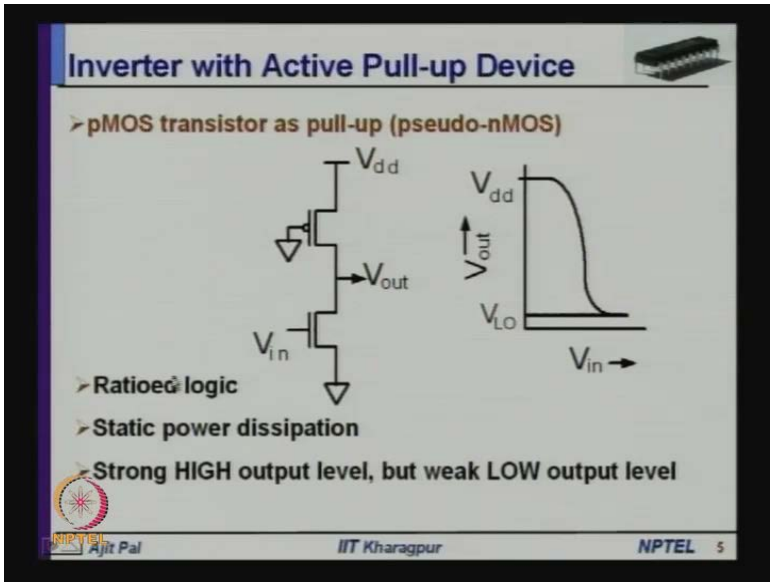

We can see this is also ratioed logic. The reason for that is when the input voltage is V d d, this transistor is on, this transistor is always on. So, output will be equal to I mean will be dependent on the ratio of the resistors, resistance values of these two transistors and obviously, l by W ratio of this device and L by W ratio of this divide will decide what will be the output and as usual when this is the situation the transfer character the

switching character characteristic will not be symmetrical because the, I mean low to high level transition time will be longer because it is this resistance of the p MOS device has to be at least four times that of the n MOS device, N MOS pull down device.

So, this is also, this will have this will have symmetrical transfer the switching characteristic and also there will be static power dissipation static power dissipation because of current flow from V d d to ground when the output is low level and input is equal to V d d and as I have already told, it will produce strong high level output, but, weak low level output.

So, this is a pseudo-n MOS inverter realized by using a p MOS enhancement type transistor as pull-up device. Now, I shall discuss about another inverter where an p MOS enhancement type device is used as pull-up device. But, the the interconnection is little different.

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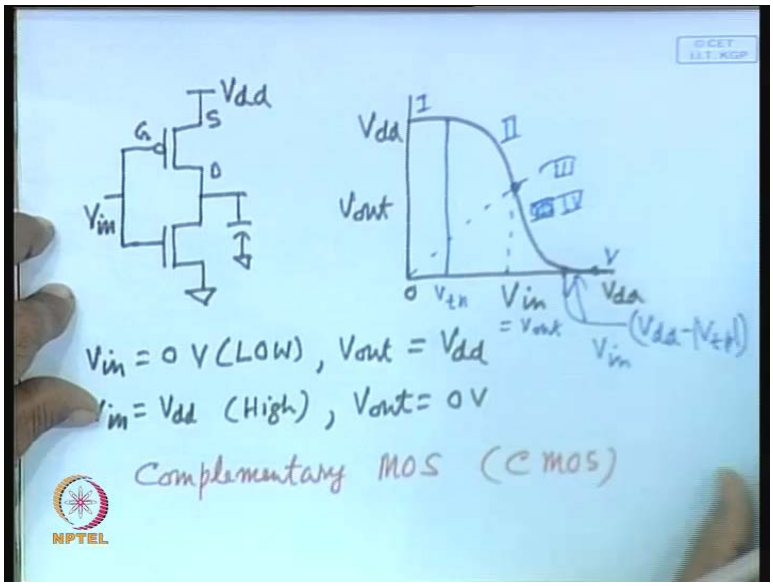

Let me draw it here. So, you have a p MOS enhancement type transistor and as usual n MOS depletion depletion type device as pull down device and this is connected to V d d this is connected to ground. Now, we have seen the limitation of this device. Here, when the input was high this was on and this was off. Now, is there any way by which we can put this device off when this input voltage is V d d?

That means when the when the input voltage is V d d only this 1 should be on this 1 should be off. If we can achieve this then; obviously, we shall not get low level output above ground level. That means, we shall we we can get strong high low level output if this is off, this is on. This can be achieved by tying both the inputs together and applying an input voltage here and what will happen in this case? When v in is equal to 0 or you can say low logic level; then this transistor will be on because here you have applied V d d. This is the source, this is the gate and this is the drain. So, this transistor will be on because it will be getting minus V d d at the gate with respect to the source. So, this p MOS transistor will be on and you will get v out equal to V d d. So, you are getting strong V d d.

Now, let us consider the case when V in is equal to V d d and that is equal to high logic level. So, what will be your V out? So, in this particular case since this is V d d; we can see this gate-to-source voltage is same. So, this transistor will turn off because the to turn it on a negative voltage of V t p is required at the gate with respect to the source. That it is not getting as a consequence the p MOS device will be off when the input voltage is equal to high. But, this transistor will be on and as a consequence you will get V d d at the output, 0 at logic level at the output because the capacitor which is connected at the as load will get will be fully discharged through this path because this this path is now off. So, you will get 0 volt.

So, what we find? We are getting a marvelous characteristic. We are getting almost ideal operation. That means, when V in is equal to 0 volt, we are getting output voltage V d d when input voltage is V d d you are getting 0 volt. So, the transfer characteristic will be will be like this. So, that means, we are getting V d d when input voltage is 0 and we shall we are getting a 0 volt when input voltage is V d d. So, this is your V out versus V in and this is known as this particular inverter is known as complementary MOS inverter. Why it is called complementary? We have seen the operation of the two active devices is complementary. When one is on; the other one is off and vice-versa. As a consequence the name that has been given to this inverter is complementary MOS inverter or in short c MOS.

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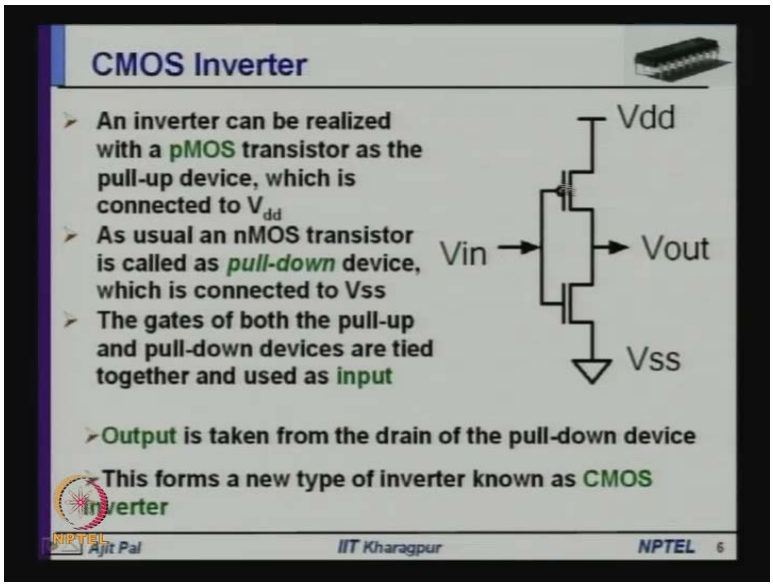

And so this is the c MOS inverter and I have already explained the operation of this c MOS inverter. Whatever is written here as I have already discussed.

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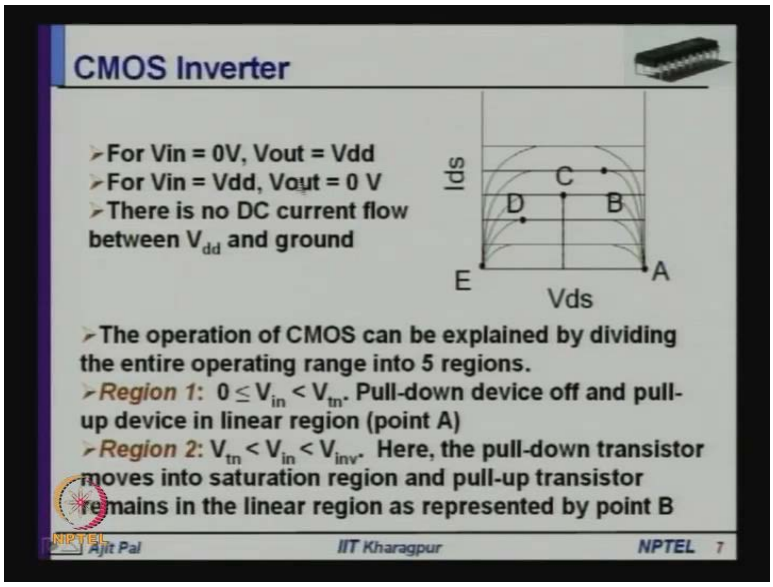

Now, let us consider the, discuss the operation of this inverter in more detail. Reason for discussing the operation of this inverter in detail is, as I have already told in my first lecture c MOS is the technology of choice. Why it is technology of choice will be clear even from the operation of this c MOS inverter. So, let us go into the details of this c MOS inverter.

Now, the operation of c MOS can be explained by dividing the entire operating range into five regions. So, to analyze the operation we shall divide the operating range into five distinct regions.

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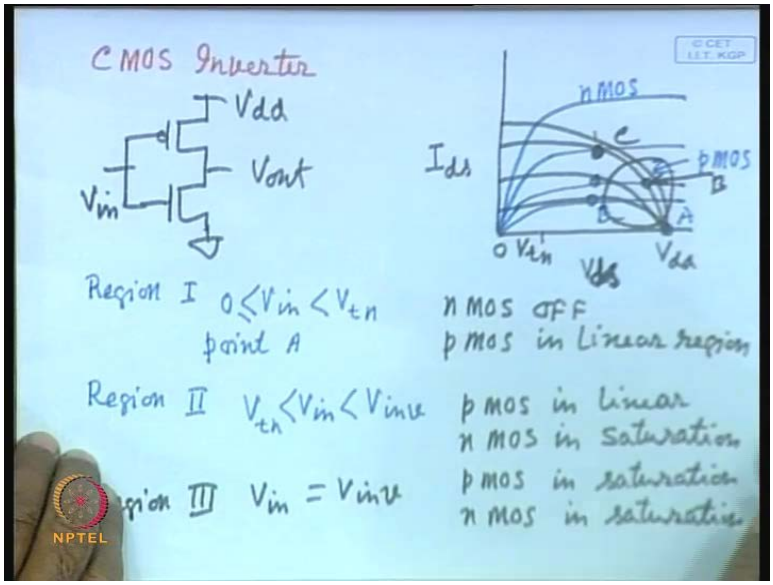

So, let let us start with region 1 and so let me draw I have already drawn the transfer characteristic. Let me draw the the current voltage current characteristics. So, we are applying input voltage here and here the current that will be flowing through the device that is particularly the n MOS transistor is shown.

And as we know, this can be obtained by imposing the voltage current characteristics of the n MOS device with that of the p MOS device. This is the voltage current characteristics of the n MOS device. Now, we can plot the voltage current characteristics of the p MOS device on the same curve, same plot. So, this is your V d d input is V d d. This is 0 here and here some current is flowing through this path. Now, we shall discuss the operation by dividing the operating range in five different regions. First, let us consider region 1. This is we are discussing about c MOS inverter.

So, in the region 1 it is assumed that V in is equal to V in is equal to greater than equal to 0 but, less than V t n. That is the let that is the threshold voltage of the p MOS transistor. Let me quickly draw the inverter here for better clarity. So, we have got an inverter here and this is the ground this is connected to v d d this is your v in and this is your v out. So, input voltage of this n, the t n is the threshold voltage of the n MOS transistor. So, what

will be the operating condition of these two transistors when the input voltage is less than the threshold voltage? That means, somewhere here.

So, this is your t v t n. What will be the condition? Input voltage is less than the threshold voltage. So, in this case what current it will will flow through this device, through this path there? As you know this transistor will be on, this transistor will be on and this device will be off. What will be the state of this device? what will be the state of this device.

This device will be in saturation. Why it will be in saturation? Reason for that is what will be the output when input voltage is 0 V d d. So, the voltage across the p MOS transistor is V d d. As we know when the voltage across a n MOS transistor is small; then the device is in saturation sorry in linear in in in linear region. We know that the the V V d s has to be less than V g s. V g s has to be less than less than V d s minus V t. That means, input volt is small device is in linear region and when it is saturation region the V d s has to be large we know that. So, based on that we can say that n MOS is off p MOS in linear region. So, what will be the output at this particular, what will what will be the point at this particular in in this particular case?

So, this is your V I have written wrongly here. It has to be what will be there what will be here V d s not V in, but, V d s here it has to be V d s. So, it it is V d s. So, operating point is this one; a. You see as I was telling that p m Vs these are the curve corresponding to pMOS and these are the lines corresponding to n MOS as I told; these line, these green the blue lines on the black lines corresponding to p MOS. You can see the p MOS device is in linear region here and the pull-down device is off. So, operating point is a. So, point a represents the represents the operating point.

Now, let us switch to region 2. In region 2 your input voltage is greater than V t n, but, less than V inversion voltage. We have already discussed about the inverter threshold voltage when V in is equal to V out. So, V i n V is equal to is is the point where v in is equal to V out. So, we are, that means, we are reaching more or less close to half of the voltage. So, when the input voltage is between V t n and V inversion it will be somewhere here. Say, this is the point B or it can be somewhere here B.

So, depending on you know it is varying within this range; so it will be somewhere here in the middle. So, in this particular case what will be the state of the p MOS and n MOS

devices? As you can see, there is a, in this particular case both the transistors are in saturation or we can say that initial part, if it is initial part the the p MOS device will be in linear. We can say the p MOS device remains in linear condition in linear because it is actually we are we are discussing about this range, not not exactly this point. This point we shall come region three, linear and p MOS remains in linear region and n MOS in saturation. We can see these are, I mean voltage is higher. So, in saturation.

And current is passing through the device current will be passing through the device and what about region three? In case of region three; your voltage V in is equal to V i n v. So, this point, the middle point any point here will correspond to this. That means, it will be somewhere here. So, we can say this is B, let us assume this is B and this is c this point. So, V in is equal to V inversion. Input voltage is equal to output voltage. In this particular case now both the devices are in saturation because here we can see this this is straight line, this is straight line; that means, the current is not changing and so the we can say p MOS in saturation and n MOS in saturation.

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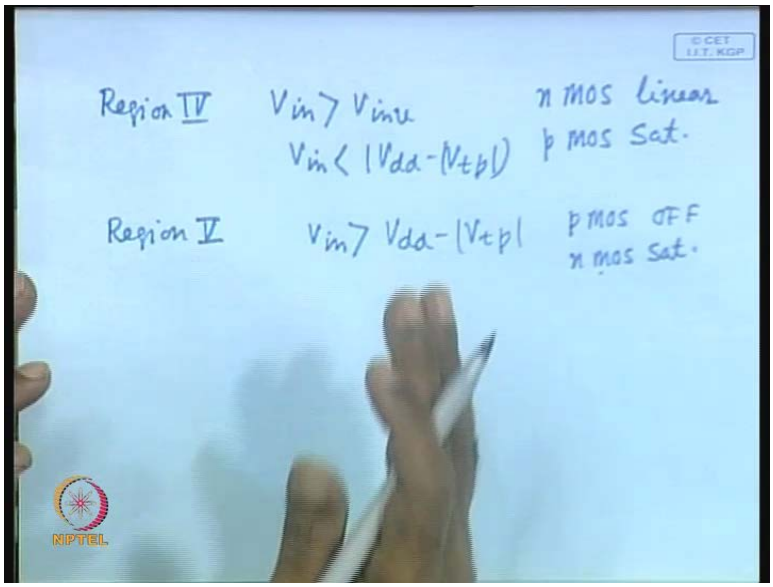

Now, let us consider the move to the region four. Region four region four will correspond to the voltage at which the V in V in is actually region four V in is greater than V in is greater than V inversion. So, let me instead of writing in this way inversion, but, V in is also less than V d d minus V t p. So, we can consider that it is somewhere

somewhere here somewhere here. That means, in this particular case V in is greater than we are moving in this direction. So, it is it is somewhere here.

So, this this particular point where V d the output voltage will be very close to 0 not 0, but, it is the output voltage is equal to V d s is equal to V d d minus V t p absolute value of V t p which is the threshold voltage of this p MOS device. So, in this case what will be the state of these devices? What is the state from this curve? We can see n MOS is in linear, n MOS is operating in linear region and p MOS in what condition? In saturation region. It has moved to saturation because the voltage is close to 0. So, voltage across this device is high, large. So, this is the source this is the drain for this transistor. So, voltage is higher for this. So, this will be in saturation, but, voltage is small for this device. So, this is will be in linear region.

So, p MOS in linear sorry n MOS in linear and p MOS in saturation region. So, this is the region four and then finally, region five. Region five when the input voltage is greater than V d d minus V t p so, what will happen in this case? In this particular case, we can see the voltage is such this transistor will be on because input voltage is above the threshold voltage of this device. But, this transistor will turn off because the voltage difference is smaller than the threshold voltage of the p MOS transistor. So, gate is less negative. I mean it is less negative than V t p.

And as a consequence this transistor will turn off and we shall get the operation where p MOS off and n MOS. In which state it remains? it remains n MOS linear region? We can say we have as if we have moved to somewhere to this point. I mean current will become 0. Now, I mean voltage is 0. So, we have moved to this point c. We can say this is the d d we can say this is E this was D this is E.

So, we can say p n MOS is saturation. So, we this is the how the, this is the characteristics of this device. Now, let us consider we have intuitively discussed the operation of the transistor in three different regions, five different regions and the transfer characteristics will be somewhat like this and how it will change if the input voltage is changing you can see this is the point this is the point which is equal to V t n.

Threshold voltage of the n MOS transistor before this this was off. So, you are getting V d d here and this is the point, this is the region. This is your region 1, this is region 2 and this is region three where V in is equal to V out. This is the point where V in is equal to v

out and then this is region three. This part and this is finally, region 1 2. This is three, this is four actually. This point was three, this this is this region is four and this is five. So, these are the five different regions and V t n here it is v v v in is equal to V out and this region will correspond to voltage when V in is V in is we have seen in the region four what was the situation.

In region four it was greater than inversion voltage, but, V in is equal to less than V d d minus V t p. So, it is greater than V inversion voltage. This is the v inversion voltage, but, less than V d d minus V t p when it transfers to somewhere here. So, this is your V d d minus V t p. V t p is a negative quantity. So, we have put absolute value and so this is the point and after that the, this transistor will turn off. So, output voltage will be 0 because this is on. So, this are these are the different points of operation of the device. Now, question is what will be the nature of current flow? Let us go back to to region 1 region 2.

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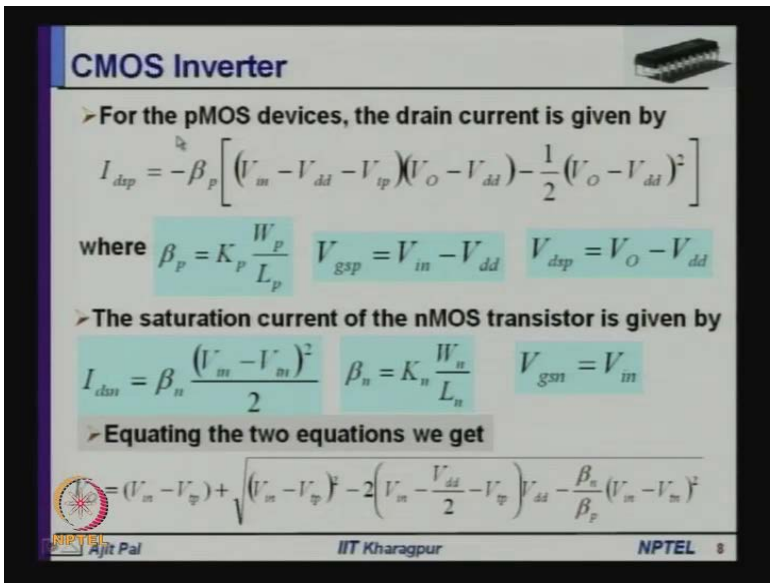

In region 2 we have seen the p MOS device; the drain current we can write this because what was the condition in the in in region 2? In region 2, your which device was on? p MOS was in p MOS was in linear so this is the expression for linear current and this this is your beta beta is K W by L which is here. So, we know that this is the expression for drain current when the device is in linear region and the n MOS device in saturation. So,

saturation current is beta n V in minus V t n square. That is your that is the by 2, that is the saturation current of the n MOS transistor.

And equating these 2 we can get an expression of the output voltage V is equal to V in minus V t p root V in minus V t p square minus 2 into V in minus V d d by 2 minus V t p into V d V d d minus beta n by beta p into V in minus V t n square. So, we can see the output will vary in this range as we have already seen output is changing. Output output voltage will be changing in this range. V output is changing as the input is increasing in this particular range in the region 2.

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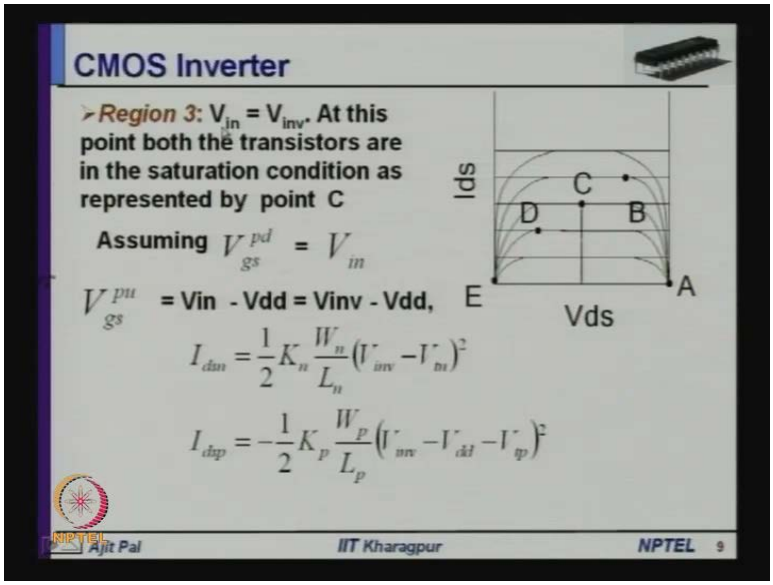

Coming to the region three; V in is equal V inversion and at this point both the devices are are in saturation. So, these are the saturation currents. This is the saturation current for the n MOS transistor, half K W by L in into V inversion minus V t n whole square and similarly, the for p MOS transistor will be the then current will be I d s p is equal to half k W by L p K p W p by L p V in V inversion minus V d d minus V t p square. So, this is the gate voltage actually is correspondence to this. So, this is this is actually the V g s and this is your V t p and here actually V d s is equal to v inversion because you are applying V in is equal to v out. So, V inversion is the gate-to-source voltage.

So, this is the expression for drain and source current.

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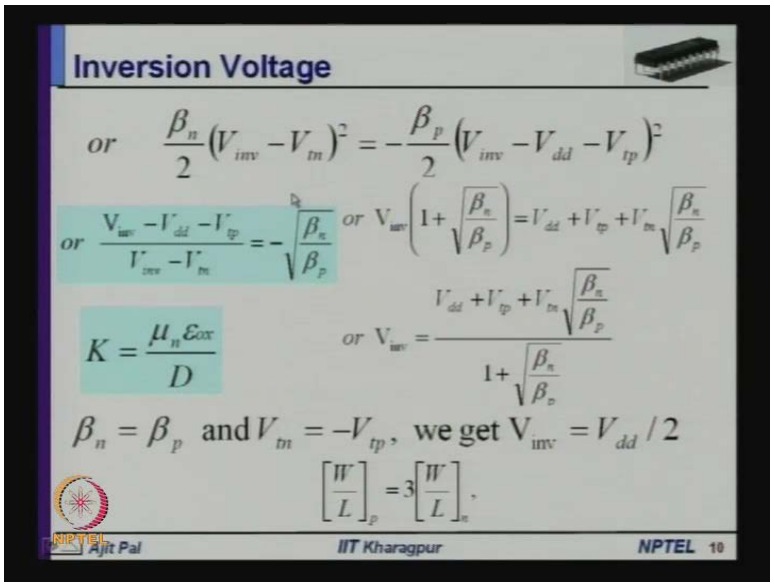

And you can equate them because you know they are in series. These two currents will be equal and by equating them we get an expression for the inversion voltage V i n V. V i n V is equal to we can see these two are equated where we have substituted V in is equal to V inversion and we are getting V inversion is equal to V d d plus V t p plus V t n root beta n by beta p by 1 plus root beta n by beta p. So, this is the expression of the inversion voltage. I mean inverter threshold voltage, inversion voltage your inverter threshold voltage you can say.

Now, let me write down this expression for little better clarity.

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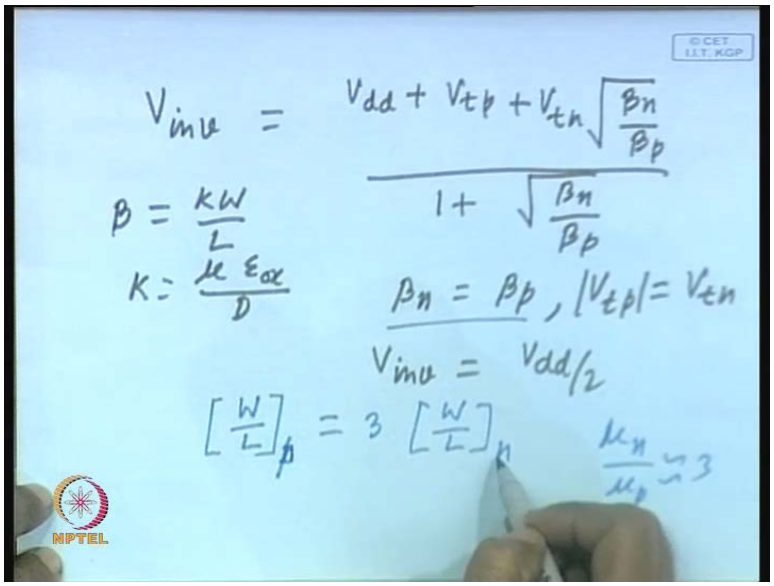

So, we are getting that inverter threshold voltage for c MOS inverter is equal to V d d plus V t p plus V t n root beta n by beta p by 1 plus root beta n by beta p beta is equal to K W by l and as we know K is equal to mu e o x epsilon o x by D. These we have already discussed in detail while discussing the characteristics of MOS transistors.

Now, in this is the inversion voltage as you can see it is dependent on several parameters. It depends on the threshold voltage of the two transistors and also the the k w by l. That means the width and length ratio of the devices and also the mobility of the devices because k will k will contain the parameter mobility. So, mobility of the devices; that means, of the transistors; that means, mobility of electron in case of n MOS transistor and mobility of hole in case of p MOS transistor and width by length of the two devices.

So, let us consider a situation where we want beta n is equal to beta p. This is what we want and also let us assume V t p, absolute value of V t p is equal to V t n. So, we are doing some simplification. We want a kind of symmetrical characteristics and to do that beta n has to be equal to beta p and the threshold voltage of the two transistors will be same of course, their polarity will be different.

So, whenever we substitute this, what what do we get? V inversion now is equal to V d d by 2 because these 2 will this 2 will cancel out. So, in the denominator we shall get 2 and since this is a negative quantity this will cancel out with this beta a beta t p is minus and this is plus. So, it will be we get we shall get V d d by 1 plus 1 2. So, we shall we are

getting V d d by 2. So, what what this condition really represents? What we really mean by this condition? If we substitute these values K p W p by L p for beta n and beta p and K n W n and by L n for beta n and then value for K, if we substitute then we shall get a relationship for satisfying this condition is W by L for the n MOS transistor or say p MOS transistor let me write should be equal to three times that of W by L of the n MOS transistor.

Actually this three is equal to mu n by mu p. That is the that is close to three. That is what is coming here. So, it will be W by L if we substitute these parameter values then we shall get mu n by mu p here W L by W p W l w by L by for p is equal to three. W by l of n transistor. So, we find that whenever we want an inversion voltage equal to V d d by 2; that is in the middle then they are the devices will not be of the same dimension. That means, the p MOS transistor has to be wider. That means, if l is same than the width of the p MOS transistor has to be three times that of the n MOS transistor.

Intuitively this can be explained very easily. Actually by making the device wider we are reducing the resistance to compensate for the lesser mobility of holes. So, we are compensating the mobility of holes by providing a wider path. So, resistance will be 1 third. So, this is the relationship and actually we can plot it later. We shall see we can plot it here.

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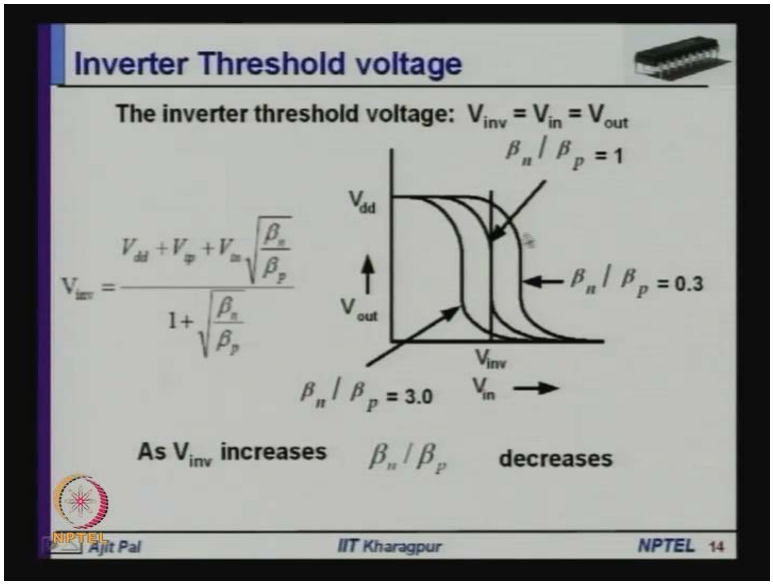

This we have plotted. Inverter threshold voltage we have plotted we can see this is in the middle where beta n by beta p is equal to 1. But, whenever the device dimensions are same that is beta n by beta p is 3; in that case as you can see inverter threshold voltage will not be equal to V d d by 2, but, it will be less than that.

Similarly, if beta n by beta p is 0.3; that means we adjust the dimensions in such a way that beta n by beta p; that means, width of the p MOS device is 1 third. So, in that case of the, that of the p MOS device is 1th of the, that of the n MOS device then we the inverter threshold voltage will move towards right. So, inverter threshold voltage can be controlled by adjusting the W by L W by W by L ratio of the two devices.

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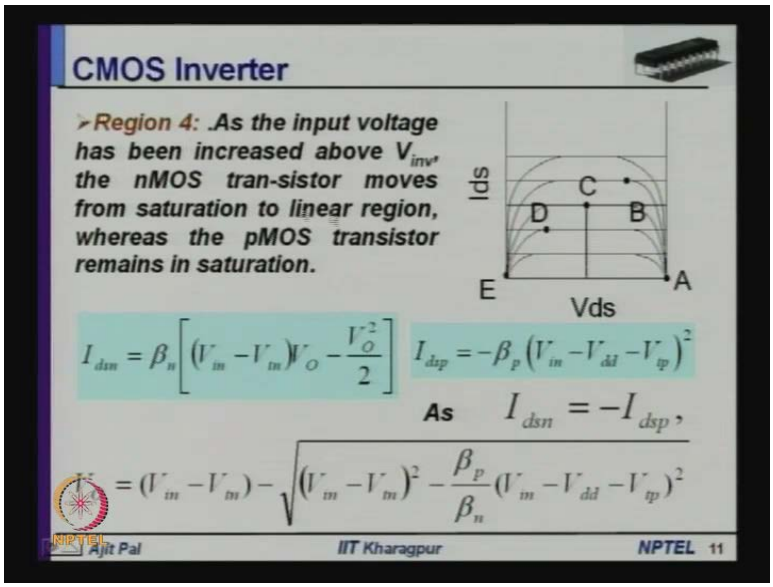

Now, in this particular case another important characteristic is the region four where again the voltage will vary, you can see the output voltage is equal to V in minus V t n minus root V in V in minus V t n square minus beta p by beta n into V in minus V d d minus V t p square and we have already seen how the output varies in this region when it is in region four as the input changes, output varies. So, this is the, this particular expression actually shows how the output varies with the variation of input. Other parameters are constant beta n beta p v t n V t p. These are all constants only parameter that will be varying is V in and how output varies with V.

And region four, I have already discussed.

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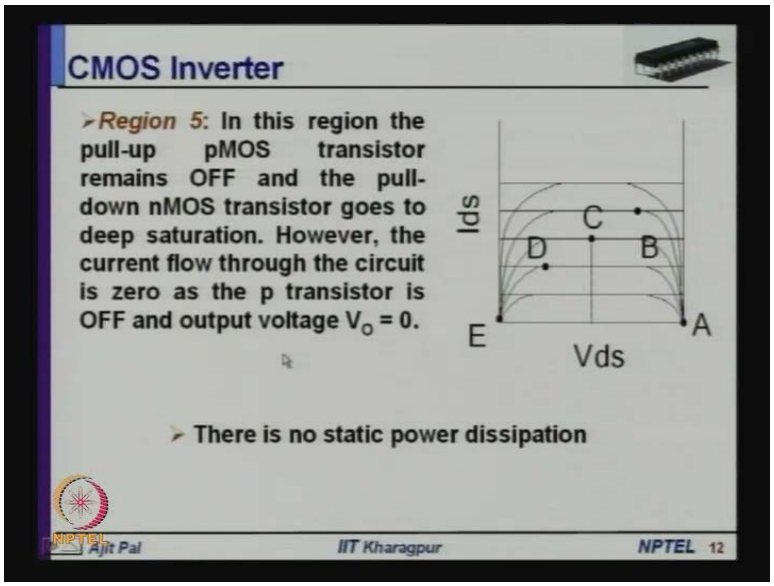

Where 1 of the p n MOS transistor is on, p MOS transistor is off. So, in this case one point that you have to notice that there is no static power dissipation. Why that there is no static power dissipation? We can see when input voltage is 0; low logic level output is V d d. This transistor is off, this transistor is on. On the other hand when v in is equal to V d d then this transistor is on this transistor is off. So, whenever we are applying two logic levels low and high only one of the two transistor will turn on and as a consequence there is no current path from V d d to ground. So, there will be no static power dissipation when the transistors are in the two different stable states low and high logic levels.

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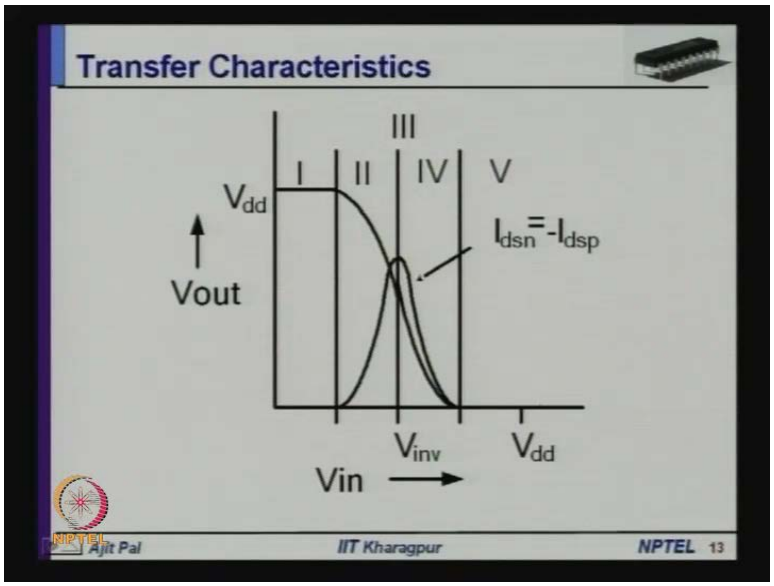

However when the input is changing from say 0 to V d d; how howhow the current will change? That can be illustrated with the help of this particular diagram. You can see as the input is gradually rising up to V in is equal to I mean equal to V t n; you can see there is no current flow and as a consequence we are getting output is equal to V d d. But, when the input voltage is greater than V t n, this is the point the when it is switching from region 1 to region 2; then you can see current is current flow has started and current is increasing until we are reaching the point V inversion and at this point the current starts decreasing until we reach the point where the point where the voltage is equal to the input voltage is equal to V d d minus V t p.

So, we can see in the middle portion when the input when the input is in the range.

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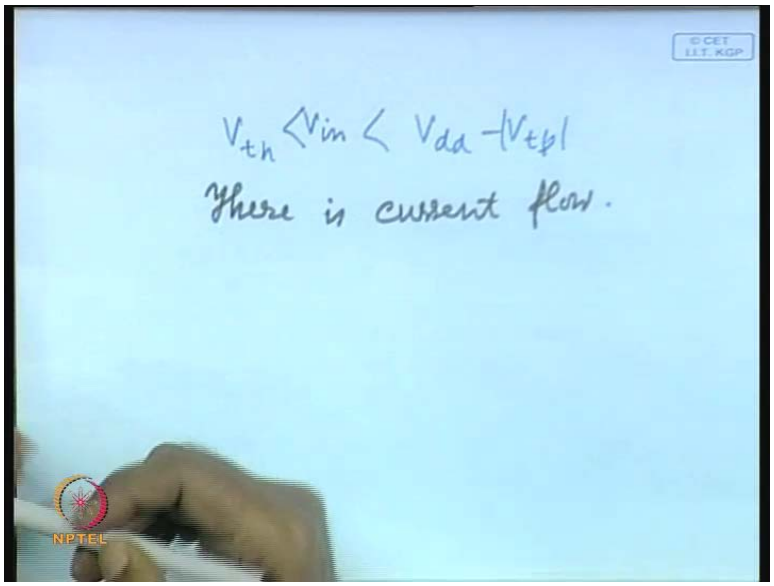

When the V in is in the range V in is greater than V t n, but, less than V d d minus V t p. Then there is current flow there is current flow. So, current flow will take place when the input will change. That means, when the input changes slowly more current will flow. But, if the change is very quick, the current flow will not be very high because that duration will be small. So, later on we shall see this will lead to a power dissipation known as short circuit power dissipation. Later on we should discuss about it because in this particular condition when the input is in this range, in this particular range then both the transistors are on and current flow will take place. That is why as if the supply voltage is sorted to ground and this will lead to what is known as short circuit current flow. Later on we shall discuss about it in more details.

We have already discussed the inverter threshold voltage.

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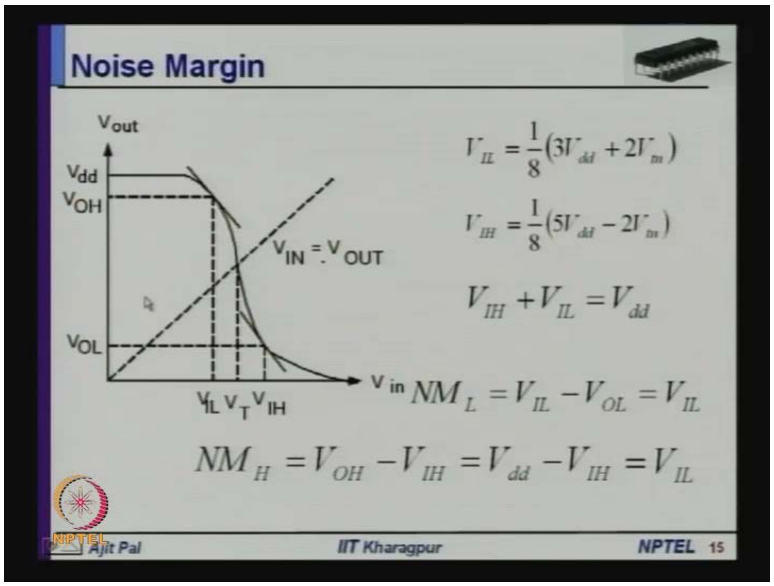

Now, let us consider a very important parameter; the noise margin which I have already mentioned in my last lecture, the noise margin of an inverter. So, ideally we can see the we are getting output voltage, high level output voltage V d d, low level output 0 and we can achieve the condition when v in is equal to v out at the middle point that is V d d by 2 that we can do. So, under this condition, the noise margin is very good because noise margin is somewhat equal to V d d by V d d by 2. But, if we take this point as the where V out V d v o by D V in is equal to minus 1 as the transition point where it is switching from high to low. Similarly, the point where it is changing from low to high that is your again slope is D V o by D V in is equal to minus 1.

If we consider these point, we can find out i l that low level voltage, this is the V i l corresponding to v o h is which can be, which is equal to it can be derived 1 by eight into three V d d plus 2 V t n and V i h is equal to 1 by 8 5 V d d minus 2 V t n. So, this particular derivation you can do and it is available in (()) book and as you can see if you add these 2 V i l plus V i h which is equal to V d d. Now, the low level noise margin n m l is equal to V i l minus V o l is equal to V i l. Similarly, high level noise margin is equal to V o h minus V i h is equal to V d d minus V i h is equal to V i l. So, we find that the noise margin of c MOS inverter is very good.

Now, let us consider another very important point that is supply voltage scaling. How the c MOS inverter will behave as we scaled down the supply voltage keeping the threshold voltage same.

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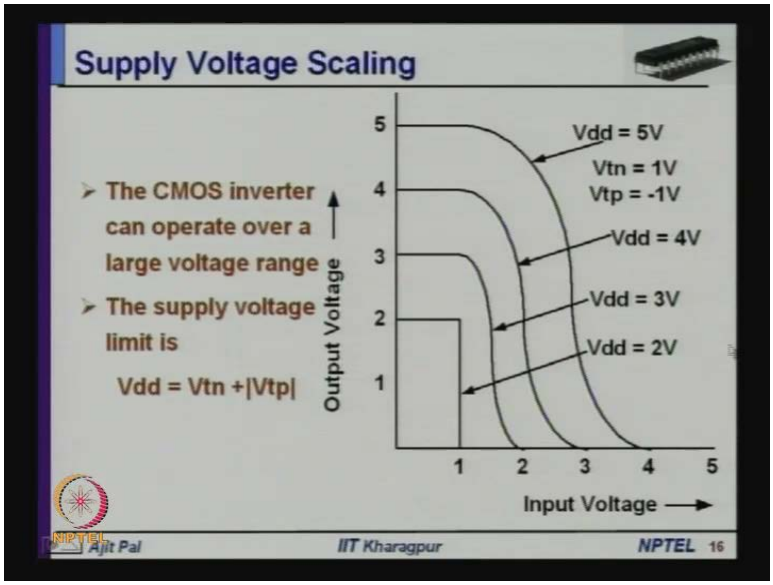

So, these are the different characteristic curves. Obviously, the transfer characteristics curves for for the five different situation when the input voltage is I mean when V d d is equal to five volt and threshold voltage is equal to 1, V t n is equal to 1 volt, V t p is equal to minus 1 volt. You can see this is the characteristic. So, this is a normal operation similarly, it will also behave correctly when V d d is equal to 5 volt, supply voltage is reduced to four volt. Similarly, this is the characteristics when V d d is equal to 3 volt, but, when we reach the point V d d is equal to 2 volt. That is a sum of V t n inverse V t p we are getting you are getting a curve like this. We can see here the transition is served. So, it switches from 0 to 1 and 1 to 0 without any flow of current.

So, there will be no current flow as it is switching from 1 to 0 and 0 to 1. So, V d d will be equal to that is why the supply voltage limit is considered to be V d d V t n plus V t p. Question arises; will the device work if the supply voltage is less than V t n plus V t p? Still it will work.

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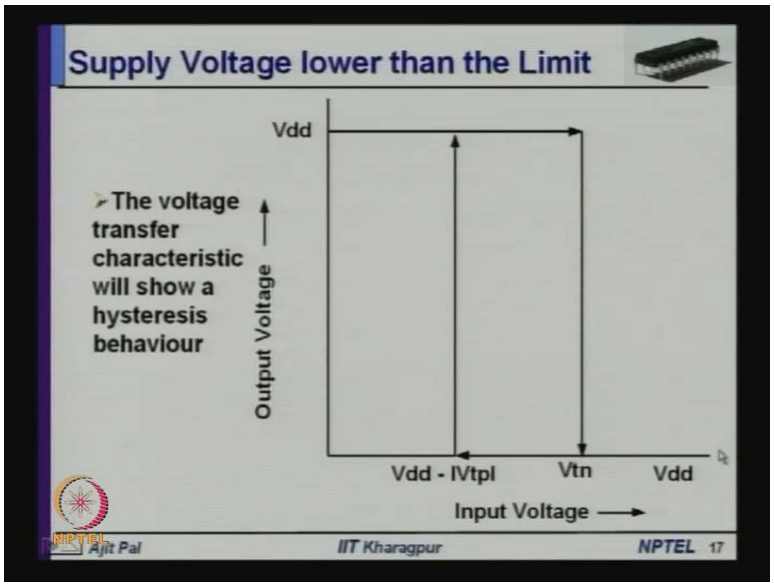

As you can see only difference is depending on whether it is changing from 0 to 1 or 1 to 0; it will move in this way. If the input is changed from 0 to V d d it will follow this path. it will follow this path On the other hand if the input changes from high level to low level it will follow the other path this path.

So, you can see there is a kind of hysteresis that will happen in the transfer characteristics when the input when the supply voltage is less than V t n plus V t p. But, I have not discussed about the delay characteristics. Later on we shall discuss about that. Although the c MOS works for very low supply voltage, but, delay will increase dramatically. Later on we shall discuss about it and low low supply voltage is necessary to reduce the power dissipation. Later on we shall see power dissipation is proportional to V d d square. So, everybody will be tempted to to reduce the supply voltage such that the the power dissipation is small. But, that will increase the delay.

Later on we shall discuss about it in more detail. And in my next lecture, I shall summarize the, I shall compare the operation of these, the different types of inverters that we have discussed in two lectures; previous lecture and this lecture. Thank u very much.