Low Power VLSI Circuits and Systems

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Lecture No. #06

MOS Inverters-I

Hello and welcome to the first lectures on MOS inverters. As I mentioned in my first lecture that it will be, we shall discuss various aspects in a bottom using a bottom up approach. So, in the last four lectures I have discussed various aspects of MOS transistors starting from fabrication characteristics and then various issues related to MOS transistors and MOS transistors switch. Now, we shall discuss about MOS inverters.

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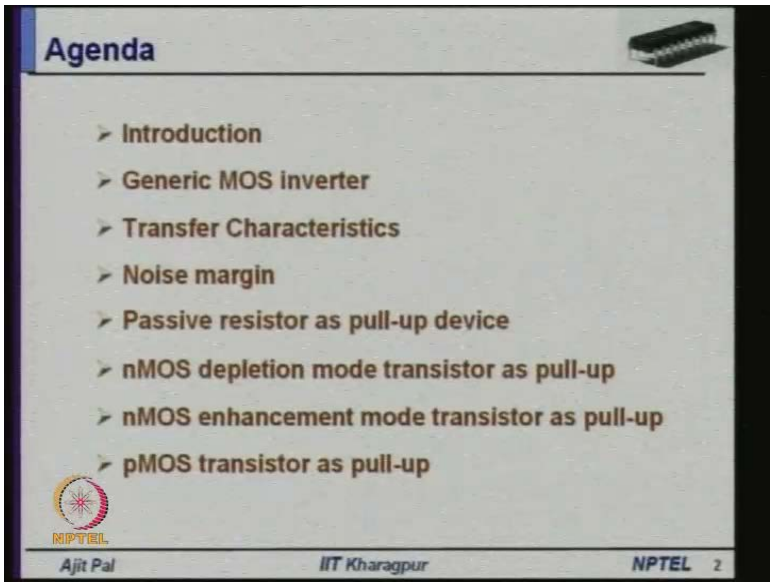

And here is the agenda of today's lecture. After giving a brief introduction about what do you really mean by inverter we shall consider a generic structure of a MOS inverter. How we can realize MOS inverter. Then discuss two important characteristics; one is your transfer characteristics and another important feature is noise margin. And then we shall discuss about the realization of MOS inverters using different approaches. Number

one is passive resistor as pull-up device, n MOS depletion mode transistor as pull-up device, n MOS enhancement mode transistor as pull-up device and p MOS transistor as pull-up device.

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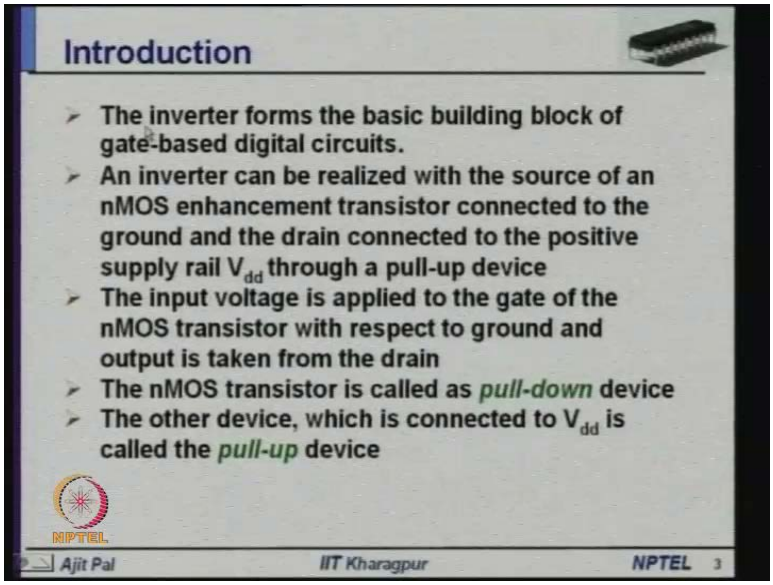

As you know the inverters forms the basic building block of gate-based digital circuits. You you must notice the word gate-based.

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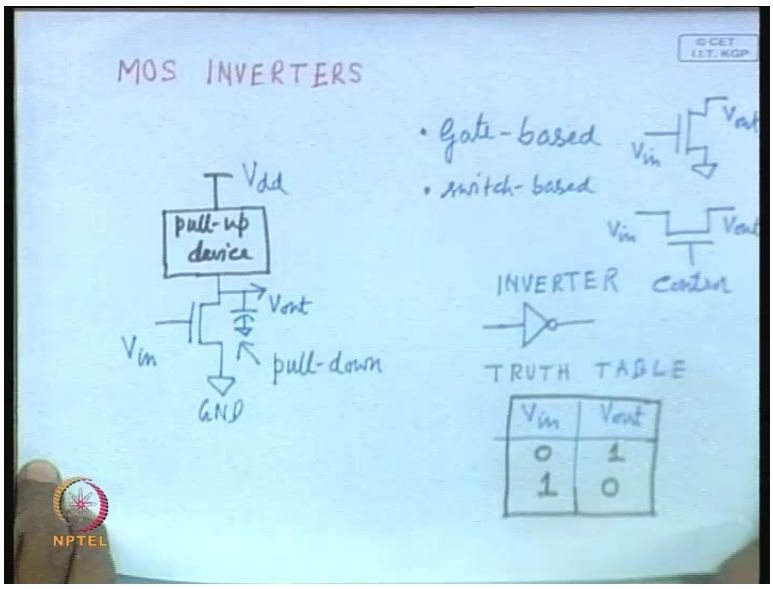

Actually MOS circuits can be of two types; number one is gate-based in gate-based circuit what you do you apply a signal to the input of to the gate to the gate and take the

output from the source. Usually I mean drain usually the source is grounded. This is one and another approach that I have already discussed when we considered MOS transistor as a switch. There we have seen that signal that you are applying. We are not applying it to the gate we are applying to to the source or the drain and gate is being used as a control circuit. I mean with the help of gate we control it. Another is gate-based and second one is switch-based. In this case, we usually apply as I as you have seen here it is your input, here also it is V in and you take the output from here and here this is control circuit. We apply the control signal here to control the resistance of this transistor and we take the output from here.

So, this is your switch-based logic, another is gate-based logic and later on we shall discuss about the use of MOS MOS transistors based on switch-based logic. For the time being we shall focus on the realization of MOS inverter which is essentially based on applying input to the gate as you can see here. Now, how you can realize a MOS inverter an inverter can be realized with the source as an source of an n MOS enhancement mode transistor and the which the source is connected to the ground and the drain connected to the positive supply rail V d d through a pull-up device. So, the general structure will be somewhat like this. You will have what is known as pull-up device and we will also have a pull-down device which is essentially a n MOS transistor and here we shall apply input to the gate of the n MOS transistor and we shall take the output from the drain of the n MOS transistor this is your V output.

Now, in this particular structure, this this n MOS transistor is called as pull-down device pull-down device and the upper one is called pull pull-up device and as we shall see the pull-up device can be realized in a number of ways. That is why I have I have not written any I may have not drawn anything any transistor anything, but we shall see what are the different alternatives available. You may be asking why you are giving the name pull-up device pull-down device the reason for that is as we shall see it will be associated with a capacitance at the output. That means, with the help of pull-up device you you pull the voltage up to the V d d level on the other hand with the help of, that means, when the pull-up device is on, then the this capacitor charges through this pull-up device rather the voltage is raised to V d d level through this pull-up device. And obviously, as you know the the MOS transistors are voltage control devices, the pull-up devices also it be device will be a voltage control device or it may be passive transistor as we shall see later and

this is the pull-down device with the help of which whenever this n MOS transistor is on you will pull the voltage down to ground level because this is ground.

So, this is the basic structure of AC MOS inverter. We have a pull-up device, we have a pull-down device and some capacitance is associated to the output of the inverter and as I mentioned the input voltage is applied to the gate of the n MOS transistor with respect to the ground and output is taken from the drain and as I have told n MOS transistor is called pull pull-down device and the other device which is connected to the V d d is called the pull-up device.

Now, whenever you you draw draw you draw the basic structure of a circuit irrespective of the irrespective of the realization usually we represent an inverter with the help of this logical symbol. This is the symbol of an inverter. You are familiar with it. Irrespective of the way it is realized and how do you represent it characteristics? You can represent the characteristic of a inverter with the help of a truth table because it is a digital circuits and truth table is the way by which is a manner by which you can represent the functionality of the inverter. So, truth table. So, in the truth table there will be 2 columns; 1 for V input another for V output and you have got 2 possible inputs that you can apply. One is your 0 another is 1 and when you apply 0 since this is an inverter it inverts the input. So, output will be 1 and when the input is 1 output will be 0.

So, this is a very simple uh circuit, but it is the most fundamental building block of digital circuits. So, with the help of this truth table you can represent the function of a MOS inverter or any kind of inverter because it is not only the MOS inverter you can represent the function of an inverter.

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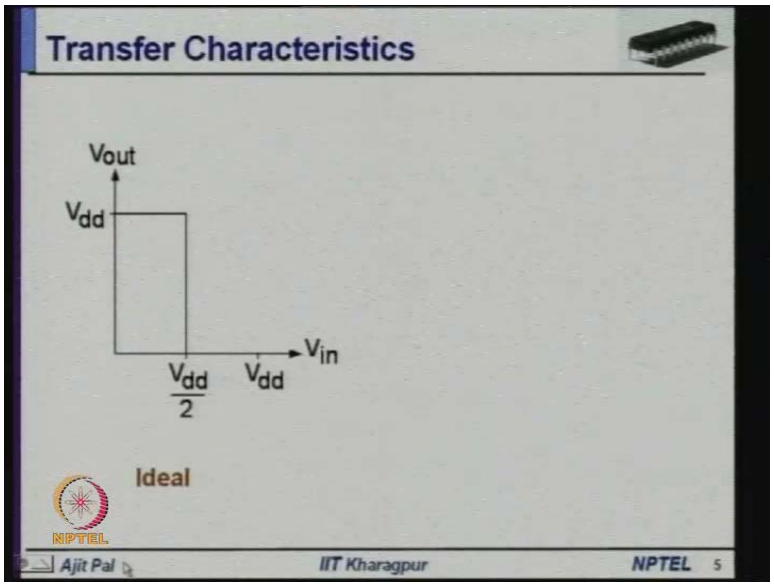

Now, we shall consider the consider a characteristic, important characteristic which is known as transfer characteristic. So, transfer characteristic of a inverter; let me draw it here.

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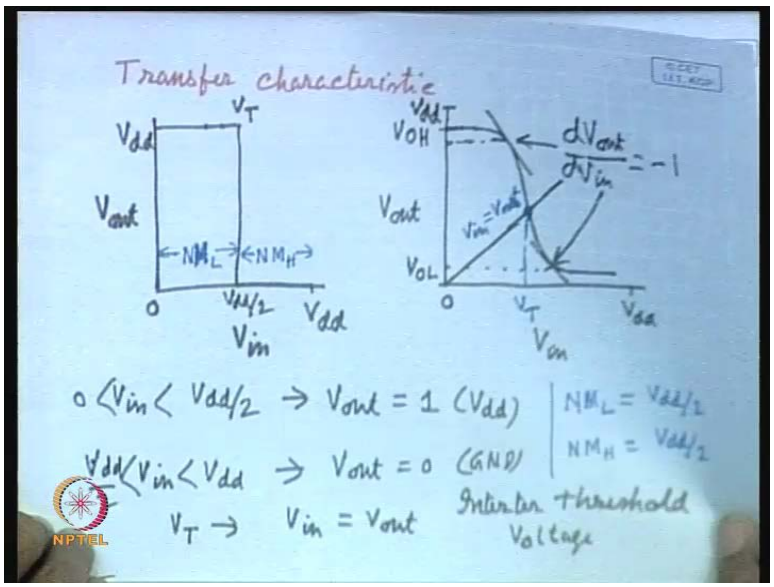

This is the transfer characteristic transfer characteristic. So, the transfer characteristic is essentially represents how exactly the output changes as you change the input. So, this is your input and this is your output. So, how the input gets transferred? I mean input changes the output, that is the represented with help of the transfer characteristic.

Ideally, an inverter will have a transfer characteristic like this. As you change the input from 0 to V d d; input will, output will switched from 1 to 0. That means, for input whenever V in is in the range of 0 to V d d by 2; V output is equal to 1. As you can see V output is 1 or V d d that is your V d d. On the other hand when the input is, V in is, V is in the is greater than V is in greater than your is greater than V d d by 2; this is your V d d by 2. So, this is in the range of V d d and V d d by 2 then, V out is 0 or ground. So, this is the ideal characteristic of an uh inverter and as you can see here the as you this input is abruptly changing at the middle. That means, whenever the input voltage is V d d by 2 and this is usually is known as V t V t or inversion threshold voltage usually it occurs whenever V in is equal to V out.

That means when V in is equal to V d d by 2; V out is also V d d by 2. That is the main feature of this V t in the ideal situation. So, V t is the uh this is the inverter threshold voltage. We have seen a MOS transistor has got a threshold voltage, but here we are we are defining a threshold voltage of the inverter. So, V t is the inverter threshold voltage and t is this is occurring at, ideally it should occur at V t by 2, but unfortunately this ideal characteristic cannot be realized by any real life inverter circuit including MOS transistor realization by using MOS transistors. So, ideal realistic situation will be different from the ideal characteristics of the inverter. So, how it will look like?

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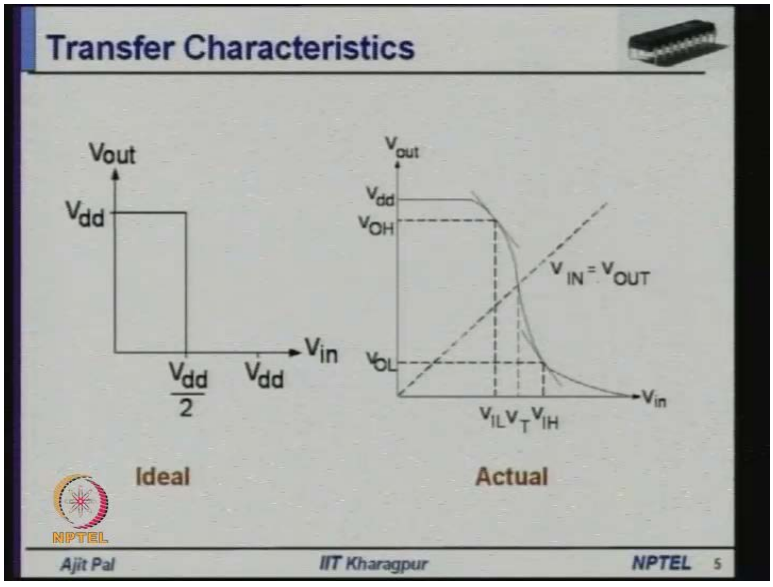

So, as you can see here; the actual characteristic is somewhat different from the ideal characteristic, we can re-draw it here for your convenience. You can see here, again this is your V in and this is your V out and input is changing from 0 to V d d and initially when the input is 0, output may be equal to V d d or little less than V d d. Why? We shall see later whenever we go for actual representation and then the, it will not really change abruptly. It will it will follow a kind of smooth curve and it will be somewhat like this. That means, this need not be suppose this is V d d. So, it may be little less than V d d. Similarly, the low level may not be exactly 0. This is actually somewhat less than less little more than 0. So, it is called the V o l output level low, this is called the V o h output high level output which is represented by this here.

Actually, this V o h and o l is also defined in some other way. You can draw a curve draw a tangent to this curve where V output sorry d v output d v input is equal to minus 1. So, where the slope is minus 1; this point represent this point represent that, this point also represent that where the where the slope is minus 1 and actually this v o h is represented by this point where it is this transition is taking place from 0 1 to 0 and it is defined by this line where d v out d v in is equal to minus1. Similarly, here this this point where d v out by d v in is equal to minus 1. So, this this region is the transition region this is represented by the V o l. So, V o h and V o l as you can see need not be V d d or 0 in real life or in actual situation.

Similarly, we have already discussed about that V inversion threshold voltage as a inverter threshold voltage. So, inverter threshold voltage also need not be equal to V d d by 2. This point where V in this is this is actually a line where which is which has been drawn where V in is equal to V output out. So, this is the point where it is crossing and this particular voltage need not be equal to V d d by 2. But this is represented as V t. So, V t in ideal situation is V d d by 2, but in practice it need not be V d d by 2. It it can be less than V d d by 2 or more than V d d by 2. We shall see on what parameters it will depend.

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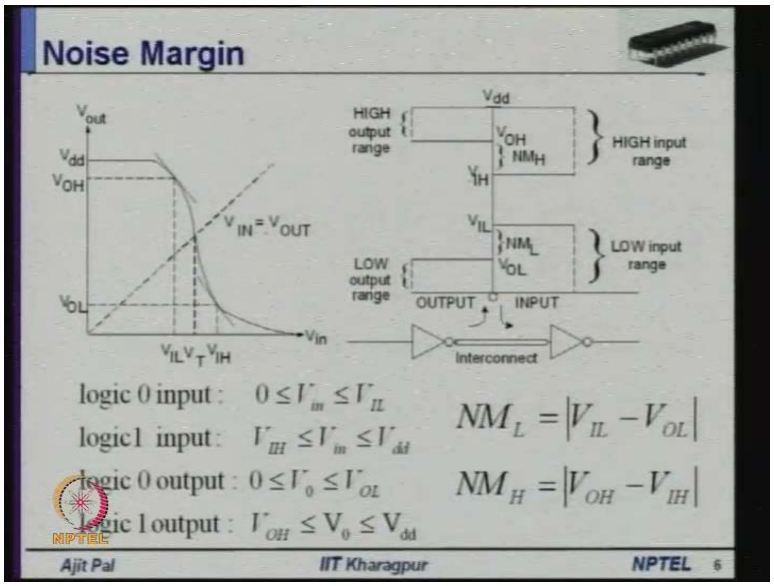

Now, after discussing the transfer characteristics; let us discuss about another very important characteristic that is your noise margin. noise margin What do you really mean by noise margin? What is the physical significance of this term noise margin? Noise margin actually characterizes the behaviour of the device in presence of noise. Whether the device will function correctly accurately in presence of noise or not that is actually decided by the noise margin factor. For example, if we look at this particular ideal characteristic there you can see the, if the input voltage is in the range 0 to V d d by 2 output is high. That means, input can change in this range. So, in this range the input can change still the output will be accurate. That means, on top of 0 volt, if there is noise and as long as the noise level does not exceed V d d by 2; the you will get correct output. So, this that is why this is called noise margin n h low that is 0 to V d d. Similarly, you can see here as long as the input voltage is in the range V d d by 2 now ideally it should be V d d. That means, in case of digital circuits we have seen that in for an inverter to get 0 output your input is V d d high.

But there may be because of the, you know some transition that is occurring in some of the circuit that will change the ground voltage. There will be noise because of industrial and various other reason and as a consequence you can see here the voltage may vary in may be little less than V d d. But as long as the voltage, input voltage is in this range V d d by 2 to V d d output will be correct. So, that is why the noise margin sorry here m sorry noise margin noise margin high. So, noise margin high you can see is also in this range.

That means for an ideal device ideal inverter noise margin low noise margin low is equal to V d d by 2 you can see 0 to V d d by 2. So, it is V d d by 2 and in case of noise margin high and the high level also it is V d d by 2. That is the ideal situation, but what about the practical situation in this case will it be will it be like this?

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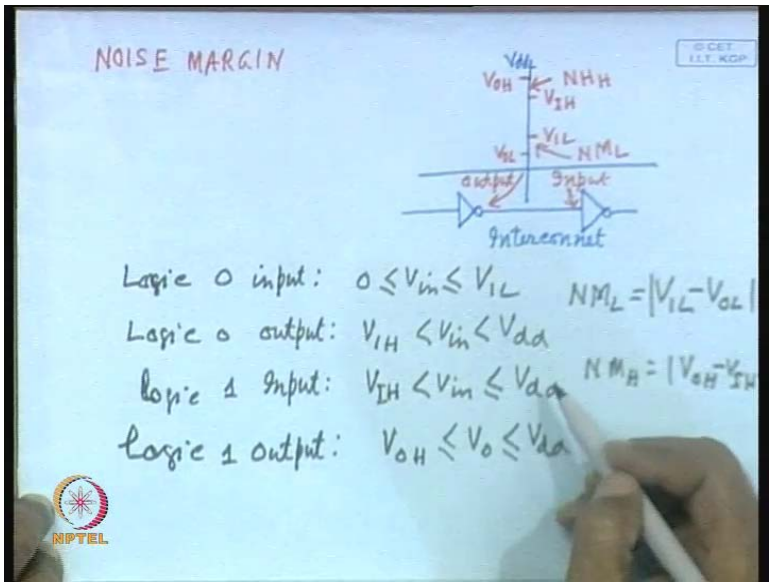

To to discuss about that let us consider let us consider a situation where you are applying the output of an inverter to another inverter. Obviously, in between you have got some kind of interconnect. Interconnect will have some resistance and here the the output will change, output of one inverter will is is being applied to the input of another inverter. So, in this case we can represent the voltage levels. For example, say this is the this is the input to the next level here and here is the here is the output of the first inverter and here is the input of the second inverter.

Now, the in using this diagram we can see that the out this is the V d d. Let us assume this is the V d d this is V d d, but we know that the output high we have already seen that output high as we can see here need not be really V d d. So, it it may be little less than V d d as you can see in a actual inverter circuit. So, we can say that this is the V o h. So, V o h that is being generated output high that is being generated by this inverter and which is applied to this next stage of inverter and this next stage of inverter you know is receiving input and how long it will function properly? As long as you can see here; as long as the input input is in this range input is in this range it will continue to function.

So, this line where this is touching it is called V i l. That means, as long as the input, low level input is in this range 0 to V i l output will be V o h. So, this V i l as long as this is the situation it will be like this and similarly we can see here as long as the input is above this this point V i h. So, V i h as long as this is input high, output will be low. It is above this V i h level, output will be high. That means, out input level if it is more than V i h then output will be 0.

So, here in here we can represent that say this is your V o h and here this is your V i h this is being applied to this input. So, V o h is generated by this stage and V i h which is required, I mean considered to be and input for high level which will produce a low level at the output, may be is little lower than that. As you can see here V o h is little lower than this. Similarly, the this V o l V o l let us assume this is your V o l V o l that is being generated by this. V o l is generated, V o l is here. V o l is generated whenever the output is low it will generate a voltage like this. But how long the output will be? I mean it will be considered as a low level up to V i l level. So, up to V i l level V i l is somewhere here. So, this is your V i l.

So, these are the inputs required for the stage and these are the outputs generated by the stage and this is essentially the noise margin; noise margin high, this is the noise margin low. Now, let us let us write down various equations for n m here this 1. So, when you are getting logic level logic 0 input logic 0 input is remains in what range? 0 less than equal to v in less than equal to V i l. This is the logic level output possible we have seen and logic 0 output is V i h V i n and V d d. In this range V i h to this range; as long as it is in this range this is the logic level output that is being produced. Similarly, logic logic 1 input is in the range of V i h V in less than equal to V d d. This is the your logic 1 input in this range V i V i h. V i h is in this range. So, this is the range V i h and logic 1 output is in the range of V o h. V o less than equal to V d d. So, you can see these are the input output characteristics.

Now, so what is your n m l? Noise margin low that is equal to V i l minus v o l. Similarly, n m h this is the range. n m h is equal to V o h minus V i h. So, this is how we can define the noise margin level low and noise margin level high. You may notice that this noise margin level low and noise margin level high will be will not be equal to V d d by 2 as we as we got it in case of ideal situation. In both the cases it will be less than V d d by 2 and as a consequence in actual implementation the noise margin that will be

getting may be less than V d d by 2 and how less that will actually decide the robustness of the circuit. How it will behave in presence of noise that will be decided by this noise margin.

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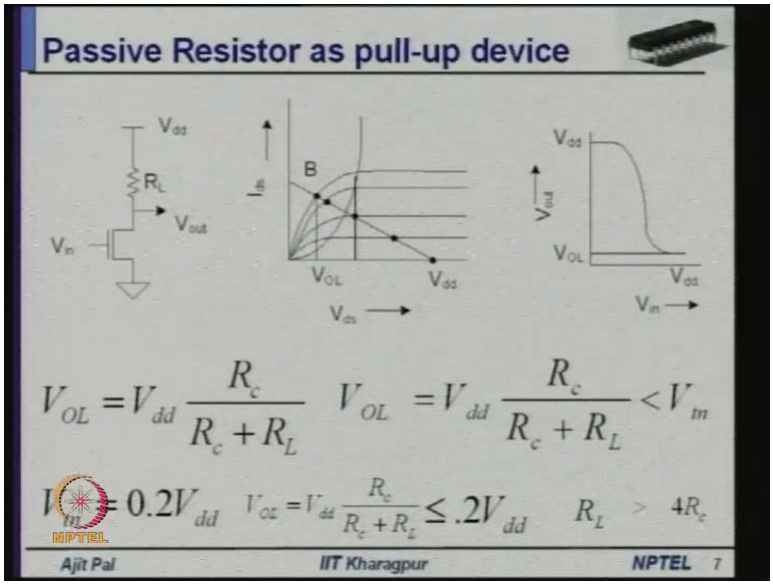

Now, let us focus on after discussing in detail the operation, I mean important characteristics of an inverter ideal and actual; let us see how actually you can realize an inverter.

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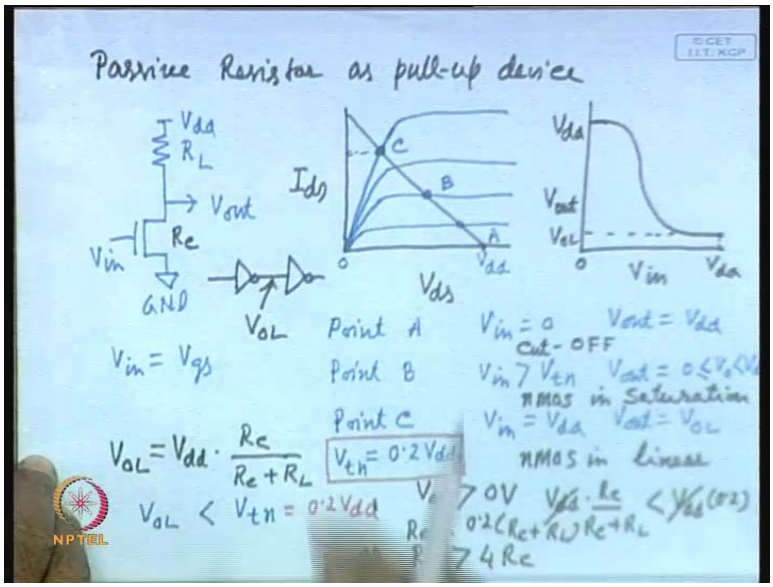

So, first we the first implementation technique is by using a passive resistor passive resistor as pull-up device. So, what you are doing in this particular case? You are applying a, you are using a passive resistor R l as pull-up device and you are connecting the n MOS transistor as pull pull-down device and so this is your V d d, this is ground and here is your V input and here is your V output.

Now, in this particular situation how the output will change as you change the input? How do you find out that? You will be interested in in characterizing the the feature, the characterizing the operation of a MOS inverter implemented by this technique. What you can do for that purpose? You can plot you can plot a curve where x –x-axis will be V d s and now the y-axis is say Y d s and you already know the characteristic of a n MOS transistor. So, it will be like this for different gate voltages, you will curve you will get curve like this and gate voltage will vary depending on the input voltage is changed here you know, V in is equal to V in is equal to V g s, gate to source voltage. What about how the output will change? To know about how the output will change, you will draw a line which is known as load line load line which essentially represents the resistance of this uh resistor load resistor that you have connected.

Now, now the the operation of the device can be characterized. You can see the input will change from 0 to V d d. Say, this is 0. Let us assume this is V d d as the input is change from 0 to V d d how the output changes? So, so when the when the lets let us start with when the input is V d d. When the input is V d d what is the output? What output will be getting? 0 because when the input is sorry when input is this; is your oh I have not drawn this is not input output characteristic as you can see when the, to do that we have to draw the transfer characteristic, but here what you are doing? You are applying the input here. So, input is changing from 0 to V d d. So, when the input is 0 what will be the output? this This transistor will be off. So, you will get output V d d. So, this point a, point a corresponds to V in is equal to 0 and V out is equal to V d d.

Then, let us consider point b. What does it represent? This is a. So, point b represents a input when it where it is where where the where the where the input is higher than the threshold voltage because the MOS n MOS transistor has started conducting. So, V in is greater than V t n. So, input voltage is greater than V t n. Obviously, point, this point this point all of them are representing that. So, in this case your V out will be equal to will be somewhere. So, it will be in the range of 0 to V o V d d somewhere in between. Now, let

us consider point C. This is point c. Point C represents when the input is V d d where when you have applied an input V d d. V in is equal to V d d. So, it is in this point b is V in is greater than V t n, but less than V d d that I have not written. So, in this case V out is equal to V o l. This is actually V o l. Ik mean this this will correspond to this point, this point will represent that.

Now, we can see how the operation of the MOS transistor is changing. So, point a corresponds to when the when the MOS transistor is cut-off, operating in the cut-off region. Point a represents when the MOS transistor is off. So, it is operating in the cut-off region what about point b? Point b you can say that MOS transistor is in saturation. n MOS in saturation. In point c, you note the it is no longer in the saturation region it is it is in n MOS in linear region linear or weak inversion region. So, as the input changes from 0 to V d d the transistor switches from cut-off to saturation to linear region.

So, we can draw the transfer characteristic as well. So, let us draw the transfer characteristic here. In transfer characteristic, you characteristic what do you plot? your How the output changes with input? So, V in and V out. So, we have seen when the input voltage is 0 then we got output V d d because this transistor was off. So, you will get the all the voltage will be dropped across this resistor. So, you will get a voltage which is equal to V d d.

Then as the input is increased; it switches, but you can see your output voltage whenever the input is V d d, output voltage is V o l which is no longer 0. That means, we can see here V o l is greater than 0 volt. That means, in this what we are observing from this realization that the whenever a passive resistor is used as pull-up device, you are getting a strong output, high level output, but weak low level output. By that what do you mean? By strong high level output we mean that whenever output is supposed to be high we are getting full high level voltage. That is your V d d. On the other hand when the output is supposed to be low level; that is 0 we are not getting 0, but little higher than 0. So, it is a we consider it is a weak low level output.

Now, you may be asking on what factor this our low level output will depend? So, on what factor V o l will depend? So, V o l how do you find out the value of V o l? So, V o l is equal to V d d into R c where R c is the channel resistance of this transistor. That means, when this is operating in this range, at this point linear range it will have some

finite resistance. So, that that since it is a voltage control device, it will have some resistor, voltage control resistor it will have some finite resistance voltage will be developed across it and that voltage I mean that voltage is output voltage and here this R l and R c together is forming a voltage divider. So, they are in series. So, what is the voltage across the R c? It is equal to V d d into R c by R c plus R l simple Ohm's law.

Question is; this low level output will you consider this low level output acceptable? How low it is? If it it is not 0; obviously, I mean how far away it is from 0? How much higher it is from 0? That you have to know and up to which point it will operate correctly. We know that the output of an the the output of this supposed to be an inverter will be applied to another stage of an inverter. So, here you will be applying V o l. You have to see whether this next stage will accept this low level as a real low level acceptable low level voltage. What is the characteristics of low level voltage? That voltage should be such that it it will not make the next stage transistor on. Then output then the output of the next stage will be high is not it.

So, what is the requirement? Requirement is this V o l should be less than V t V t n supposed to be because this is also being applied to another transistor and obviously, the output of the next stage will be high provided the input is less than the threshold voltage. So, V o l should be less than V t n. That is the requirement to be satisfied for the correct operation of the inverter. So, far as the high level is concerned, there is no problem. We are getting V d d. There is problem will low low level output. So, low level output has to be less than V t n.

Normally this threshold voltage V t n V t n is has some nominal value. Let it be 0. 2 V d d. Typically, typically the threshold voltage is is is has some relationship with the supply voltage that is equal to 0. 2 v d d. That means, if we substitute it here in this expression; that means, this is equal to 0. 2 V d d. Then what condition it it requires? I mean what is the what what is the outcome?

That means V o l in place of V o l we shall be substituting this 0. 2 V d d. That means, V d d into V c by V c plus V l should be less than V d d into 0.2. 0.2 V d d 0. 2 v d d. So, if you solve this equation. What will you get? You will get that your your V l you see V d d v d d will cancel out. So, this side will be equal to 0.2 V c plus V l. That means, V c should be less than 0.2 R c plus R l or R l should be greater than four R c. That means,

the the resistance of this. Load resistance the passive resistor that you have put has to be at least fourth times the resistance of this channel resistance R c. So, that is a that is a very stringent requirement. Without that it will not behave as, it will not operate as an inverter. It will not be it is operation as an inverter is not acceptable.

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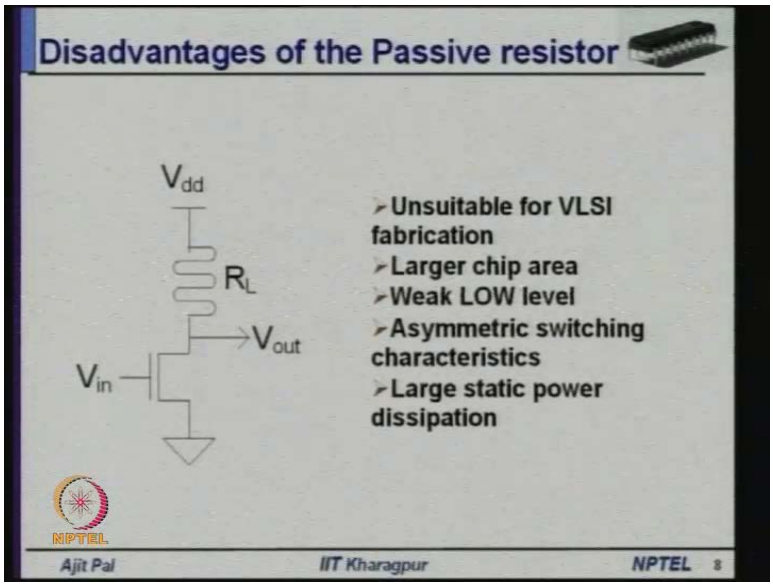

Now, based on these what are the limitations and advantages of a MOS inverter realized using passive resistor is is let us see disadvantages. First of all it is unsuitable for VLSI fabrication. Why it is unsuitable for VLSI fabrication? Whenever you try to realize a passive resistor in VLSI you you can use two possible approaches; One is diffusion based approach; that means, you will create a diffusion region isolated diffusion region whose resistance has to be equal to four four R c and obviously, it will require lots of area. Another alternative is you can use poly-silicon without doping, undopped and that that can be used as resistor. But unfortunately whenever you use the second approach it is value cannot be accurately controlled because of wide process parameter variation of VLSI technology. As a consequence, this realization of MOS inverter using passive resistor as pull-up device is not feasible and I have already mentioned, it will occupy large chip area. Either way whether it is a diffusion based realization or realization by using that poly-silicon undopped poly-silicon based realization.

Secondly it provide provides you weak low level as we have already seen the output level is not really 0. So, here you are getting a voltage which is higher than 0. So, we can

say the output is weak. Then third factor which is very important; asymmetric switching characteristic. What do you really mean by asymmetric switching characteristic? You see we have seen we shall be see we shall see later on that operation of MOS circuits are essentially charging and discharging of capacitors. So, charging of discharging of capacitors; that means, here you will be having some capacitor connected and this current has to be charged through this R l and discharge through R c. Since, R l has to be fourth times R c; obviously, this charging time will be at least fourth times that of the discharging time. So, charging and discharging times are not same asymmetric. Obviously, on time and off time or low, low to high level and high to low level transition times will be different and which may not be acceptable in many situations. So, asymmetric switching characteristic.

Fourth factor is large static power dissipation what do you really mean by static power dissipation static power dissipation is when the input is not changing then what is the power dissipation. So, here as you can see when this input voltage V in is equal to V d d in this situation. That means, input is high then this transistor is on and as a consequence there is the current will flow through this R l R c ne 2 R k and as a consequence there will be power dissipation. Obviously, the current the power dissipation will be dependent on R l and R c and here also there is a kind of V c r circle V c r circle is this this value of this resistance R l and also that of R c you want if you want to reduce it to to increase the speed of operation then the power dissipation will be more. That means, higher the speed of operation larger is the power dissipation. Obviously, it is not acceptable from low power applications and particularly the static power dissipation is not acceptable in low power applications.

So, these are because of these disadvantages this realization of MOS inverters using passive resistor is not done, it is not feasible.

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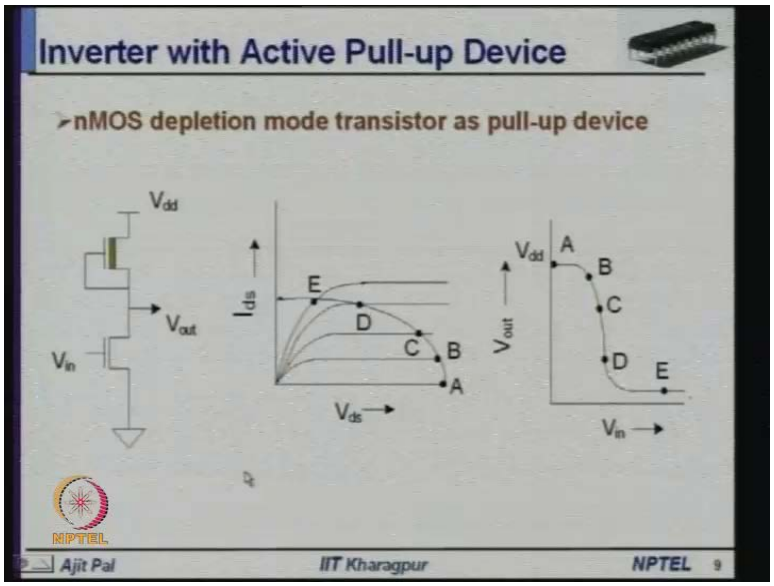

So, what are the other alternatives? Next alternative is to use active pull-up device.

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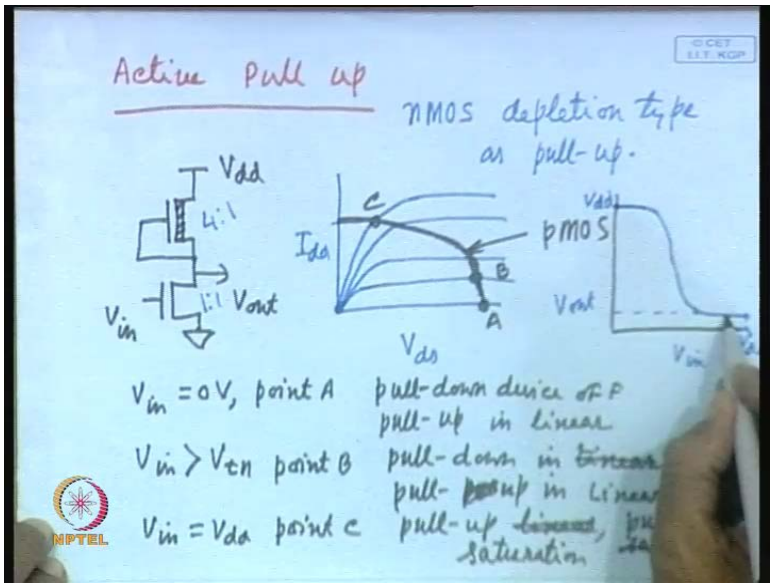

So, active pull-up active pull-up. So, whenever you say active pull-up what do we really mean? We mean that we shall be using some active device. What kind of active device will be using? Obviously, you will you will be using a MOS transistor and we have four alternatives at our disposal. That pull-up device can be a n MOS enhancement type transistor, it can be a n MOS depletion type transistor, it can be a p MOS enhancement type transistor or it can be a p MOS depletion type transistors. So, you have got four

alternatives. Let us see which alternatives are good or acceptable and which which can be used for the realization of MOS inverters.

So, let us start with first alternative that is your, that is the case where we are using n MOS depletion type transistor as pull-up device. So, what we are doing here in this particular case, we shall be using a MOS transistor as pull-up device and this is a depletion type n MOS transistor. So, when you are using an n MOS type depletion, n MOS depletion type transistor what you can do? You can connect the gate to the source. Why so? Because since this is the depletion type transistors if you connect this gate to the source it will be always on. That means, it will offer a resistance always it will offer a resistance because the gate is connected to the source and the transistor is on when gate is connected to the source. That is the basic feature of a n MOS depletion type transistor. Then you will be applying here input and you will be taking output from here v output. So, what will be the characteristic of device? How do you really obtain the characteristics of this device? What you can do?

In the same way you can plot V d s and I d s and since this n MOS transistor can operate with different gate voltages; you have to draw several lines, several curves for the n MOS transistor. But there will be a single curve for the p MOS transistor. So, this is the curve for the p MOS transistor corresponding to V g s is equal to 0. Here, gate is connected to the source. So, this corresponds to p MOS. So, p MOS is in linear region in this part and sorry in saturation region in this part and linear region in this part.

So, in this case as the input changes from 0 to V d d; how the output will behave or in what conditions this transistor will be? I mean this as well as that. So, when the input voltage V in, V in is V in is equal to 0 volt; then what will happen? This pull-down device is off. So, V in is equal to 0 volt. This corresponds to point a. Point a when pull-down device off. What about the pull-up device? Pull-up device is in linear region, you can see it is in the linear region pull-up you have to not only tell it is on. You have to tell whether it is in saturation or in linear region. So, pull-up in linear region when V in is equal to V in is equal to greater than V t n threshold voltage of the n MOS transistor then what will happen? It will move to may be this point say this point B. This is A this is B.

So, in this particular case what what will happen? the What is the operation of this transistors? Point b pull-up pull-down in which region? Linear region, in linear region

and pull-up pull-up in sorry pull-up in pull-up device is in, no here pull-up device is also in linear region. Pull-down in linear sorry this is the pull-up in pull-up in saturation sorry pull-down in saturation it is not correct in saturation here. So, it is in saturation and pull-up in linear then when V in is equal to V d d. Let us go to directly to this point that is your point C. So, here what is the condition? Pull-up is in linear linear and pull-down in saturation. Pull-down is in saturation because this part is linear.

So, we can see here as the input voltage changes from 0 to V d d; their the operation of these transistor changes. So, from the pull-down device switches from off to linear off to saturation sorry pull-up pull-down device switches from off to saturation no no no I have written wrongly. Pull-up pull-up is this one linear and pull-down is pull-down is linear sorry it will be linear and pull-up this is the pull-up in saturation I have written wrongly. Pull-up in saturation, pull-down in linear.

So, based on this we can draw the transfer characteristic as well. So, transfer characteristic can can also be drawn. What will be the transfer characteristic? Transfer characteristic will be you can see here when the input voltage is 0 what is the output you are getting? You are getting V d d. Is it not? it. So, for this V in and here it is V out transfer characteristic. So, it changes from 0 and then I mean V d d output is V d d, but as you can see the low level output is not 0 just like your passive transistor. Here output is not 0 the reason for that is when input is d d then both the transistors both the transistors are on when the input is V d d, here it is V d d both the transistors are on.

Maybe pull-up in saturation pull-up in saturation and pull-down in linear, but this is the point pull-up in saturation pull-down in linear and, but both of them will be having some finite resistance. So, they will act a kind of voltage divider and as a consequence what will happen? the the You will get a voltage which is not really 0, but little above 0. So, we are getting a voltage which is above 0 and obviously, this is non-ideal characteristic.

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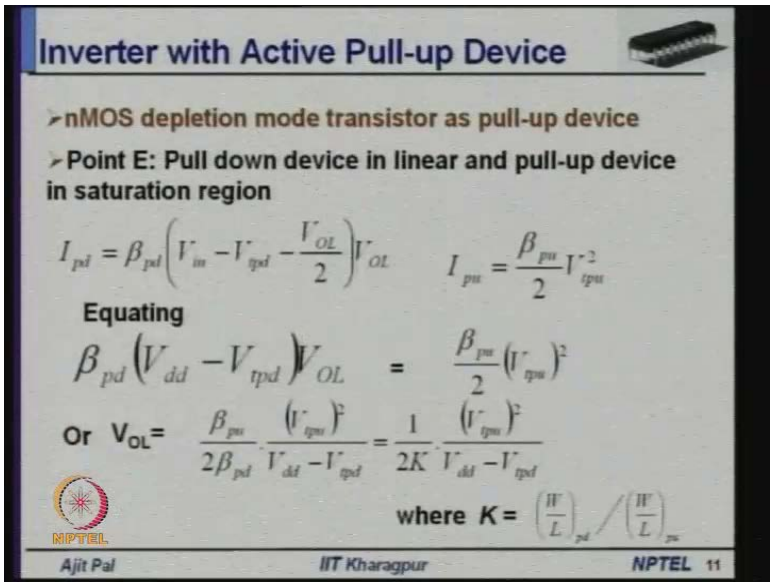

So, what we can say about its the the advantages and disadvantages?

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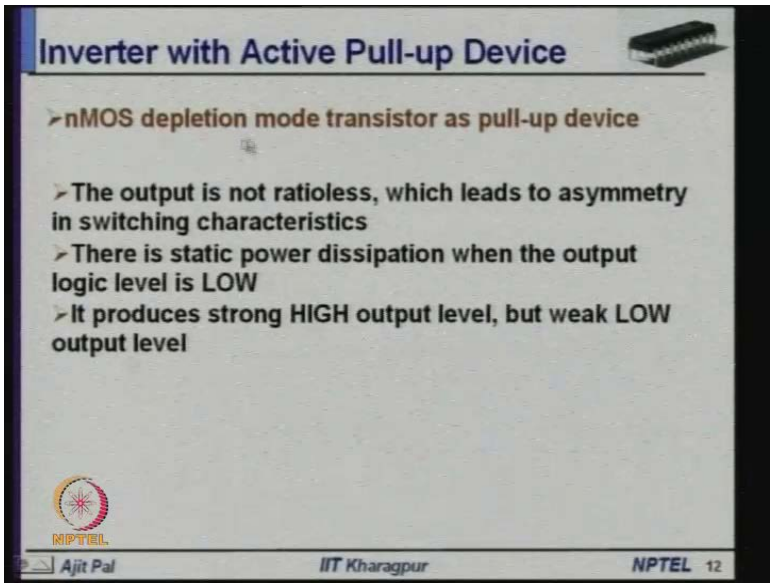

So, n MOS whenever you are using n MOS depletion mode transistor as pull-up device; we find that the output is not ratio less. What do you mean by that? You see if the output is dependent of the L by W of the ratio of the transistors then we call it it is ratioed logic. What what do you really mean by that? The resistance is dependent on the length ratio of the length and width of the device and whenever it is dependent on that; we call it ratio logic. So, this is a ratio logic because output voltage as low level will be dependent on

the resistance of the L and R. So, in this particular case as we know, this resistance has to be fourth times that of this. That means, length has to be if it is four and width is L here it has to be L each to L. That means, length of this pull-up device has to be fourth times to of that of the pull-down device and as a consequence, this is a ratioed logic and the the character output characteristics will not be symmetric just like your transistor. I mean static resistor and also there is static power dissipation when the output level is low as you have seen when the input is V d d, then output is low level and current flows through this path because both the transistors are on and there is static power dissipation and we have already seen that output level is strong, high high level is strong and low level is weak.

So, let us conclude today's lecture by summarizing what we have discussed today. We have we have introduced the basic concept of an inverter, we have introduced the characteristics of an ideal inverter in terms of noise margin and transfer characteristics. Then we have seen how you can realize a MOS inverter and we have discussed two alternatives; one using passive resistor, another is by using a n MOS depletion mode transistor. So, in in my next lecture I shall discuss about the other alternatives of of realizing of inverters where we shall see how we can realize inverter by using n MOS enhancement mode transistor as pull-up device and also p MOS transistor as pull-up device. Thank you.