Low Power VLSI Circuits and Systems

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Lecture No. # 05

MOS Transistors-IV

Hello and welcome to today's lecture on MOS transistors. This is the last lecture on this topic. Today I shall discuss about MOS transistor as a switch. In the last couple of lectures, I have discussed how MOS transistor can be fabricated and then basic structure of a MOS transistor. Then I have explained the operation of a MOS transistor with the help of a very simple model known as fluid model and in my last lecture I have discussed the electrical characteristics of the MOS transistor and I have derived expression for the drained current and you have seen what are the various parameters on which the drained current depends.

Today, I shall discuss one very important application on MOS transistor. That is transistor as a switch.

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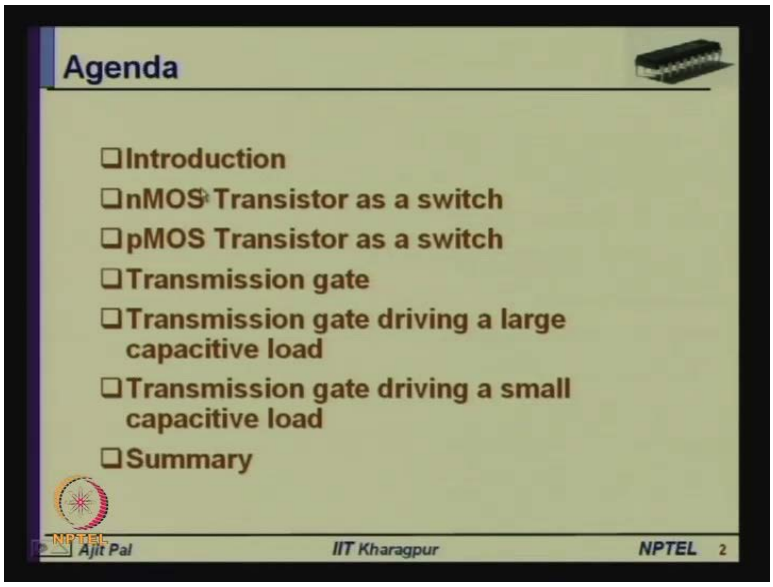

And here is the agenda of today's lecture. I shall give a brief introduction about this and then I shall start with MOS transistor as a switch. Why do you require a MOS transistor as a switch? Then p MOS transistor as a switch, transmission gate, then transmission gate driving a large capacitive load, then I shall consider transmission gate driving a small capacitive load, then I shall summarize what I have discussed.

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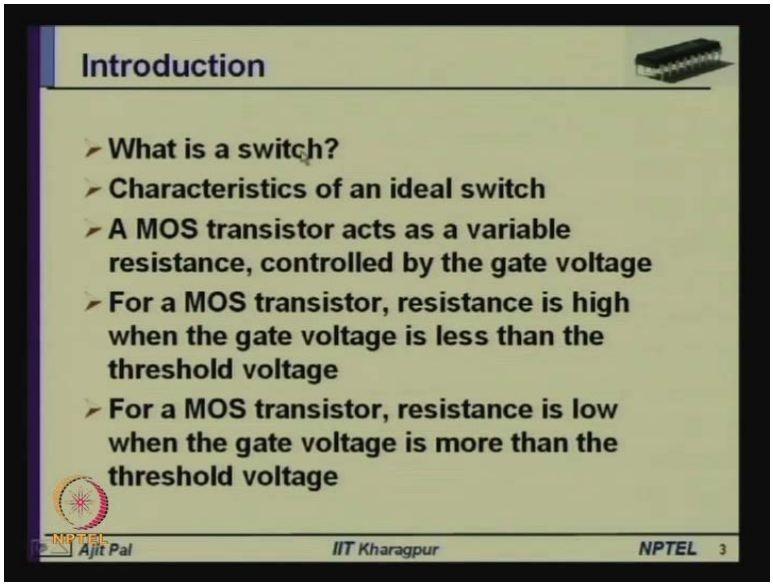

First, I shall discuss what is a switch. You may have heard of switch rather everyday you are using switch in your day to day life.

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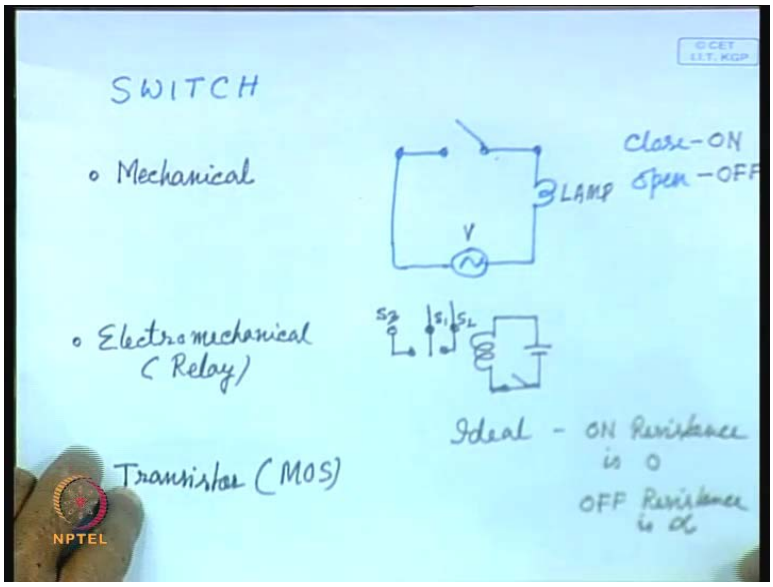

What do you really mean by switch? You see as you get up you have to turn on the light and you use a switch. Electrically it can be represented by this. So, it has got two contacts and you are taking connections. Then these connections can be connected to a say A C supply and maybe it is in series with the lamp. So, this type of switch is known as toggle switch. That means, if you push it it will be closed and whenever you push it on the other side it will be open. That means, it has got two straight close and open or you can say close is you can write is as on and off, you can also write this way.

So, this kind of switch which is known as mechanical switch, you are using in your everyday day to day life to turn on lights, fans, various types of electrical and electronic devices. And as you as you can see it has two states. There is another type of switch which is known as electro-mechanical. This is you can also call it a relay is being used in many electronic circuits. What is a relay? It has got a magnet, electro-magnet and switches. There is one middle point. You can see there are three contacts I have shown and if you pass current; obviously, you have to pass D C current because it is a relay and whenever you pass current through it, this particular middle contactor is attracted to this. That means, these two lines will make contact and whenever no current is passed through it, so that means, you have got you can say another switch that can be a, in fact, electronic switch or some mechanical some of those type of switch, but, the current passing through is not very high, but, here the current than can be passing through it can be very large.

So, this is a relay as you can see; it has again got three contacts; middle one, then this side; that means, whenever this electromagnet magnet is energized these two lines say S 1 and S 2 makes contact. And whenever this is not energized, then S 1 and S 3 makes contact. Here also it has got two states again, on and off if you are using these two can be used for connecting some electronic circuits like say geyser or some oven or anything of that kind which can be controlled electronically. So, this type of switch is very popular.

Now, today; obviously, we shall be discussing about the use of another switch that is transistor as a switch that too MOS transistor. Now, whenever we go to use the MOS transistor as a switch, before we do discuss that let us consider another very important aspect. That is characteristics of an ideal switch. So, whenever we say switch, it has some characteristics ideal, non-ideal. What do you really mean by an ideal switch? Say whenever we close it, then current passes through it and whatever is the voltage say this

is your v that is that is applied across this lamp you can say. Now, whenever we consider a switch is ideal; when the on resistance is 0 on resistance is 0; that means, whenever it is put on there is no resistance, it does not offer any resistance. So, the whatever voltage you apply that is that is applied across the lamp there is no voltage drops across the switch.

So, an ideal switch does not degrade the signal that is the characteristic. On the other hand if it is similarly, whenever it is off, then resistance is very high or I mean ideally infinite, but, even when if it is very high will serve the purpose. That means, off resistance should be infinite. So, whenever these two characteristics are satisfied we call it an ideal switch and obviously, in such a situation whatever signal is connected through the switch will not be degraded or distorted. The signal will reach the load. In this case lamp is the load without any degradation or distortion.

So, this is how we define an ideal switch and obviously, whenever it is non-ideal on resistance in real, in in reality anything will have some finite resistance. That means, whenever it is on it will have some finite resistance and whenever it is off that resistance may be very high, but obviously, it will not be infinite. So, that will be the situation of a practical switch. Obviously, we shall see how the MOS transistor behaves in terms of these ideal characteristics.

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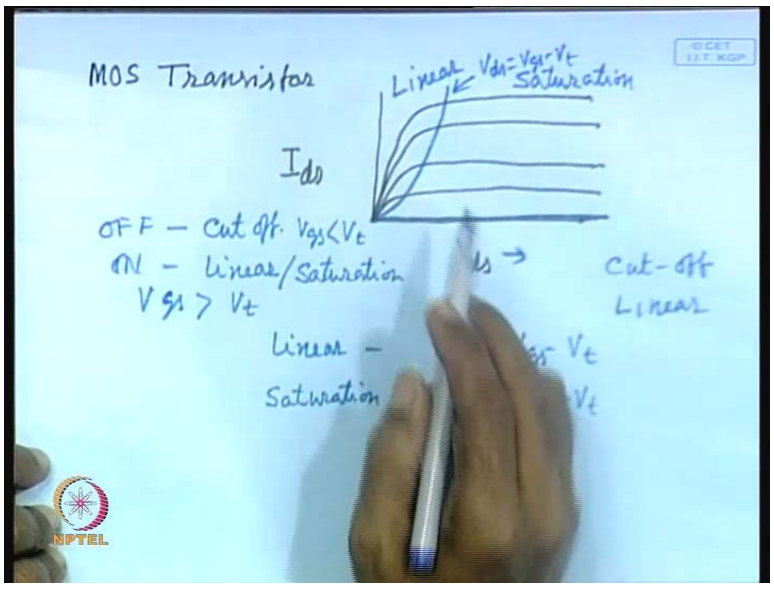

We have already discussed the, we can say MOS transistor characteristic we have already discussed. We know that it you there is a variation of drained current as you change the drain voltage and that that is for different gate voltages.

So, these are the different gate voltages and as we know there are three modes; number one is your number one is your cut-off. Then this line represents that cut-off region when there is no current passing through it. Then we have seen there is another region that is your linear and finally saturation. So, this is your saturation region. We have already discussed that. So, we have to understand whenever we try to use MOS transistor as a switch, where it will operate? In which mode it will operate? At which point it will be operating when it is off or on? Obviously, when it is off it will be in the cut-off region. That means, MOS transistor is off, it will be cut-off and whenever it is on, it may be in linear or in saturation. On which factor it depends? That means, whenever the MOS transistor is on; it will be either in one of the two states; linear or saturation. On which factor it will depend? It will depend on the voltage across the device. That means, V d s as you have seen if V d s the voltage across it is less than V g s minus V t then, it will be in the linear mode linear or non-saturated mode. On the other hand, it will be in the saturated saturation mode or saturated mode whenever V d s is greater than V g s minus V t.

So, this line, this is the line this is V d s is equal to V g s minus V t demarcates the operation between linear region and saturation region and obviously, whenever you are using it as a switch, you may not have control about the voltage across it or in other words it may vary. So, it may operate, the switch may be closed by applying a suitable gate voltage. That means, whenever it is on it will be made on by applying a gate voltage which is greater than V t, threshold voltage and off means the gate voltage is, that means, V g s is less than V t. And on means V g s is greater than V t. But, the operation will depend on the value of the V d s, drain to self-source voltage and as we shall see later whenever this transistor is on, it may, it operation will vary from one mode to another mode. It will may switch, it it may go from linear to saturation or saturation to linear and. So, on it it will depend on the application.

Then as as you already know for a MOS transistor resistance is high when the gate voltage is less than the threshold voltage as I have already told. So, this is in this mode it and it is used as a off state of a switch and for a MOS transistor resistance is low when

the gate voltage is more than the threshold voltage which I have already mentioned. That means, whenever it is on.

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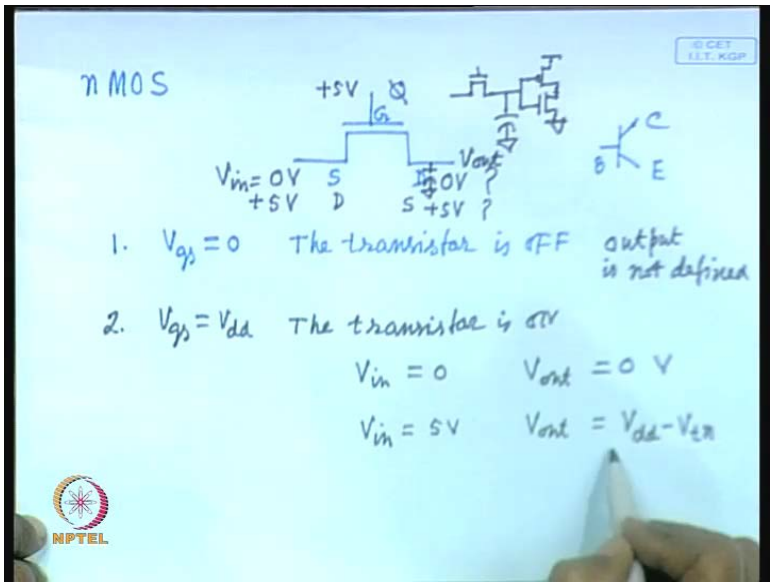

Now, let us consider the use of n MOS transistor as a switch. So, n MOS transistor can be represented by this. Here one point you must notice; even not applying input to the gate. Gate is used to control the operation of the switch you are applying input to one of the two terminals source or drain and in case of a MOS transistor one very interesting factor is the transistor, I mean the source and drain are perfectly symmetrical. That means, any one of the two terminals can be used as source the other one can be used as drain unlike you know bipolar transistors. In case of bipolar transistors you cannot really interchange you know that that emitter and collector. There's an emitter collector and emitter cannot be interchanged their operation will be different. But, in case of a MOS transistor we have already seen the structure and from the structural view point we have seen the physical structure is identical and as a consequence later on we shall see same terminals some some time sometimes it is operating as a source and other point of time it is operating as a drain as we go for discussing the operation of a MOS transistor.

So, whenever here you are applying let us assume whenever you apply 0; then whenever the V this is your V g s. That means, first let us consider when V g s is equal to 0 gate to source voltage is 0. Obviously, we assumed here this is the source and this is the drain and this is the gate V g s is 0. In this particular condition the transistor is off that we have

already seen is off. But, whenever this transistor is off what will be the output? Say suppose you have applied 0 volt here. can Will you get 0 volt at the output? Or say suppose you apply say plus 5 volt which we considered to be 1 will you get plus 5 volt? There is a question mark. Why I have put the question mark? The reason for that is you know the output is essential can be considered that there is a capacitor connected to it. Why? we This this MOS transistor may be connected to other parts of the circuit. Say suppose, it has been connected to an inverter and as we know this inverter this they are connected to the base and they they are having capacitance. So, we can say here there will be load capacitance C L and obviously, C L will hold the charge and the output will be dependent on what was whatever was the input before it was turned off. That means it is acting as a kind of memory. Output does not fully depend on the present input.

Just prior to closing of putting the switch off; whatever was the input that output will be available as you turn it off and in fact, this property can be used to realize memory devices using MOS transistors. In fact, the dynamic RAM that is may that is that is realized is there precisely it is used in this way. That means, the intensive capacitor is used to hold the information. So, that is the reason why here whenever V g s is equal to 0 the transistor is off, but, output is not defined. Not defined means it depends on the previous state. So, since it acts as a memory.

Now, let us consider the case whenever V g s is equal to V d d. That means, you have you have applied instead of 0 you have applied say plus 5 volt V d d, supply voltage. In this case what will happen? In this case the transistor is on. transistor is on Now, transistor is on, but, what voltage you will get at the output? Will you will you get 0? Or you will get more than 0 or less than 0 depending on the previous state? You see you are applying plus 5 volt here and this is 0 and obviously, this transistor will always remain on. I mean irrespective of the output. So, this 0 I mean if this capacitor was let us assume earlier there was a voltage plus 5 volt here and it will discharge to 0 eventually. It may take some time because of the finite resistance of the transistor. But, in the steady state output will become 0. That means, if V in V in is 0; then V out V out is also 0 volt in the steady state. That means, the as we can see the low level voltage since we are concerned about you know digital circuits your our input is high or low 0 or 5 volt.

So, this 0 level, low level is passing to the output without any distortion whenever the input voltage is say 5 volt what about V out? yes. So, output you see this here 5 volt.

Here 5 volt. Here you can see the role of this these two terminals has reversed it is no longer source you can consider it as drain and this as source. So, since this is a this is 5 volt and initially may be this is 0. So, this transistor is on, but, as this capacitor output capacitor see charges gradually it will reach the point where the voltage will be equal to V d d minus V t. It is the threshold voltage of this MOS transistor. At that point this transistor will turn off. So, that means, output cannot charge beyond V d d minus V t or say V t n to signify n MOS transistor.

So, we can see here the as the input input voltage is V d d, you are not getting full output voltage it is getting degraded and output will be V d d minus V t n. That means, it will be less by the threshold voltage of the MOS transistor because at that point of time the transistor is turning off. So, here it is plus 5 volt, there it is in the gate it is plus 5 volt and here at this point it is V d d minus V t. So, if it rises further, the transistor turns off. So, you can see in case of a in MOS transistor, you are not getting the full output it is getting degraded.

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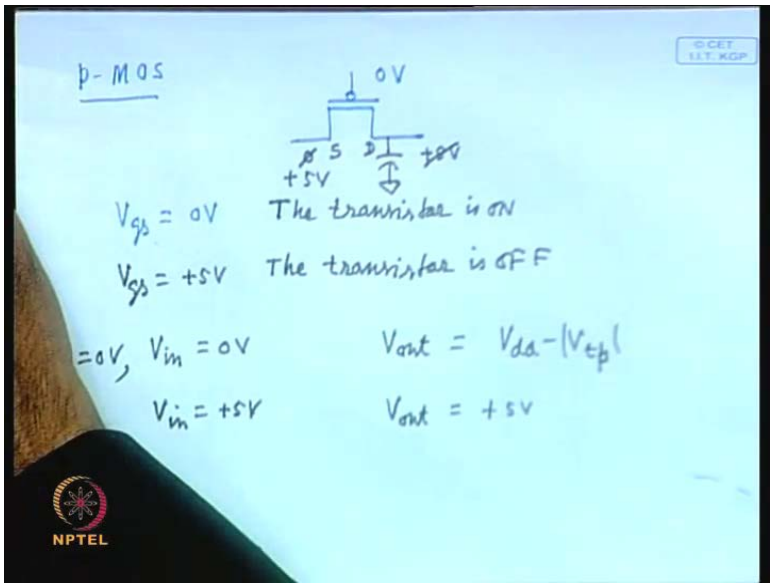

What about p MOS? Say let us now consider the p MOS transistor p MOS transistor. In case of a p MOS transistor; let me draw the diagram of p MOS transistor. This is a p MOS transistor. Now, in this case whenever you apply 0 volt then what will be the situation of this? Then the transistor is on. That means, whenever input, I mean gate V g s is equal to 0 volt; then the transistor is on the transistor is on. On the other hand,

whenever you apply V g s is equal to plus 5 volt, then the transistor is off irrespective of the inputs that you apply. Transistor is off; that means, whenever the, it is plus 5 volt then the transistor is off. So, again the transistor behaves like a, you know a kind of memory. We have already seen the output cannot be fully defined. It it does not fully depend on the present input. It depends on the past input. So, at the point of time when it was switched from 0 to 5 volt at that point of time whatever was the input that that output that input will reach the output and it will be retained by the capacitance that is present here. On the other hand whenever V g sis equal to 0; the transistor is on.

Let us see the operation of the MOS transistor when the transistor is on. That means, whenever V in is equal to 0 volt, V g s is equal to 0 volt. At that time what is V output? what is V output We have assumed that V g s is equal to 0 volt what will be the output? You see here 0 volt here it is 0 volt. So, there is no difference and initially let us assume this was plus 5. So, this source is gate is non-negative with the respect to the source. So, the transistor is on, but, how long it will remain on as the capacitor charges it will turn off whenever it will reach V d d minus V t n N t p absolute value of the threshold voltage, of the MOS transistor and at that point the transistor will turn off.

And. So, you can see here here the 0 level is not reaching the output properly that the low level voltage is getting degraded what about V in is equal to plus 5 volt. So, here instead of 0, we apply plus 5 volt. What will be the output? Let us assume initially it was plus 5 volt. You can see in this particular case this is this is now acting as a source; this is acting as a drain. And this transistor is always on because gate is non-negative with respect to the source plus 5 volt. So, the transistor is always on. That means, V output will be equal to plus 5 volt. That means, the the high level is reaching without any degradation.

So, the characteristic is exactly opposite to that of n MOS transistor. You have seen in case of n MOS transistor, the low level signal was passing without any degradation, high level was degraded. In case of p OS just the opposite the high level is reaching without degradation low level is getting degraded.

Now, can we now get best of both the words? We have seen that the n MOS, neither n MOS transistor nor p MOS transistor behaves like a ideal switch. Either low level is degraded or high level is degraded depend on the depending on the type of transistor you

are using. Is there any way by which we can get best of both the words? That means, the good features of both the transistors we try to achieve. How can we do that? We can do that by combining two transistors in parallel.

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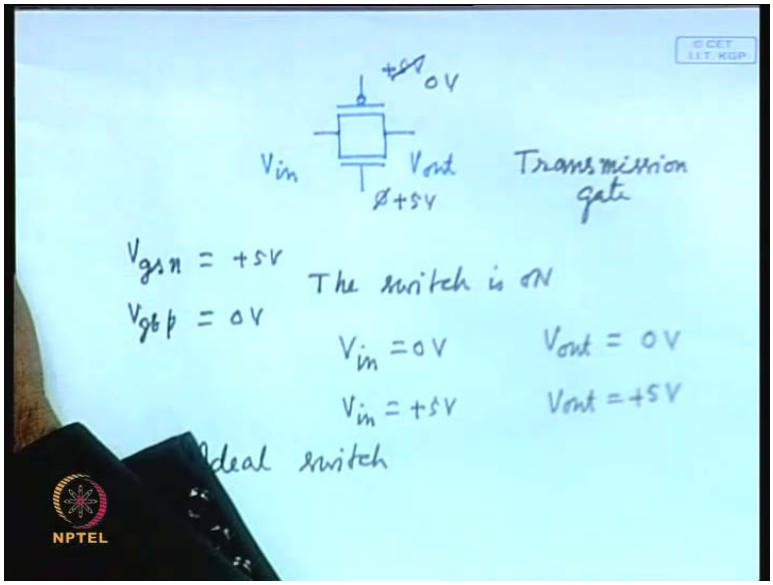

So, what we can do? We can have a p MOS transistor in parallel with a n MOS transistor. So, this is n MOS transistor and this is a p MOS transistor and this is your V in and this is your V out. Obviously, you you can turn them off by applying say plus 5 volt and 0. So, in that case it will be a, it will be both the transistors are off. So, it will behave the output will behave like your n MOS or p MOS transistor. That means, in this particular case output is dependent on the previous value.

So, as you can see we have to apply complimentary complimentary outputs into inputs to the gate gates of these two transistors. That means you have to make them simultaneously on or simultaneously off. So, in this particular case they are off. So, here the output voltage will be dependent on the previous state.

Now, to make the switch on; let us apply 5 volt here and 0 volt here. That means, V g s n is equal to plus 5 volt n MOS transistor you are applying plus 5 volt and V g s p we are applying 0 volt. That means, the switch is on. In this case, if you apply V in is equal to 0 volt what will be the output? What will be the output voltage? You can see you have now two transistors in parallel the the p MOS transistor in this particular case will not pass the 0 voltage. But, it will pass through the n MOS transistor; that means it is 0 volt. So, it is

always on. So, output will be output will be 0. That means, a low level signal will pass through the n MOS transistor without any degradation. Similarly, if you apply V d d or plus 5 volt V output will be again plus 5 volt, a high level signal will pass through the p MOS transistor without any degradation.

So, you can see now we are getting a kind of ideal switch in terms of you know, it may not be perfectly ideal, but, ideal in terms of that you are getting the low level and high level are passing without any degradation. So, and this particular device is known as transmission gate which is realized by combining two transistors in parallel n MOS and p MOS transistors and applying complementary output, complementary inputs to the gates and by that you can turn the switch on or off. Now, so far we have considered only the use of p MOS I mean different types of switches to realize, to check whether the logic levels are passing to through it out properly or not.

Now, we shall start the dynamic behaviour of the switch and we shall see whether how the current is shared by these two transistors do they share equally or you know their current sharing changes as the input and output changes. So, we shall study the kind of dynamic behaviour.

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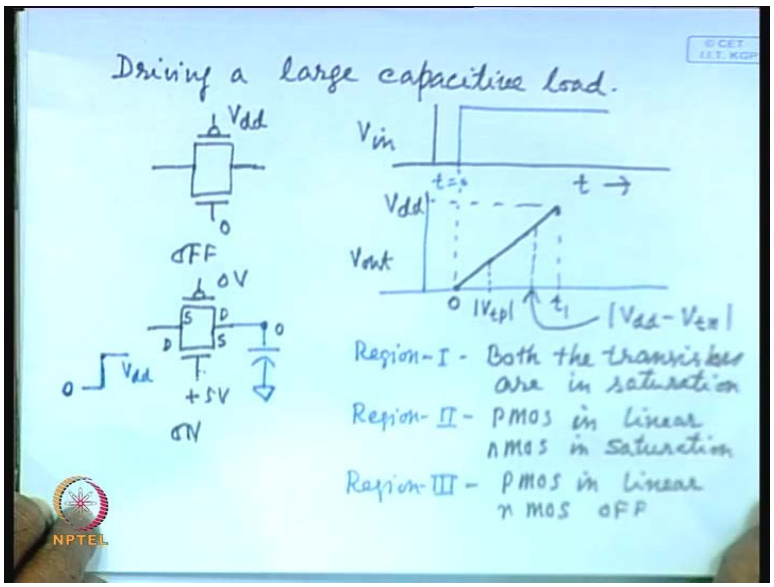

And to do that, we shall consider the switch case where the transmission gate is driving a large capacitive load. That means, you have got a transmission switch. I mean transmission switch p MOS and n MOS in parallel and let us assume, let us not bother

about the off condition. Let us assume both the sorry put the opposite way; that means, in this particular case, the output will be, it will be it will be off. Let us consider the case where we are considering the both the transistors are on. So, here you are applying 0 volt and here plus 5 volt and the transistor is on. In this particular case what we have done? We have assumed that here you have got a large capacitive load. By large, we mean this capacitor's value is relatively high compared to the intensive capacitances of the devices which is of the order of femtofarad, may be this is of the order of picofarad not femto farad. Then we consider it large pico farad may not be a very large capacitance, but, when we consider in terms of MOS, you know transistor capacitances then it is large because the intensive capacitances like gate capacitance, source capacitance these are of the order of femtofarad.

So, these are in the range of let us assume it is several pico farad. Now, what we are doing? We are changing the, we are applying a input and suddenly changing it from V d d to 0 to V d d 0 to V d d we are changing it from 0 to V d d input is instantly instantaneously changed from 0 to V d d. So, you are using a, you are applying a step input what will happen at the output? So, since this as we know this both the transistors are on. So, obviously, this assuming that initially this was zero volt it will start charging. So, we can say that the output, the capacitance. So, this is V n. Vn has changed from say let us assume this is this is the time this is t is equal to 0. At this point it has changed from 0 to 1. What about V output? What will happen? Obviously, at this point the output this is your V out and in this axis it is t. So, initially the voltage was 0. So, it will charge. It will charge, the capacitor will charge and output will gradually build up and it will go from 0 to V d d eventually. So, 0 to V d d.

So, at the output at the output goes from 0 volt to V d d during this period of time; obviously, this time will be dependent on the on-resistances of these transistors which are not zero. If the if the on-resistances were 0; it would have charged instantaneously, but, this will not happen because the un-resistances are not really zero. They have finite on resistances and the capacitor will gradually charge from 0 to V d d and during this period we shall see the condition of these transistors how they change with time from this 0 to say t 1. This is the time during which the output is charging from 0 to V d d.

So, initially what will be the condition of these two states? We can divide the operation in three regions; regions one, region two and region three. How we shall define the three

regions? Say initially what will be their states? You can see here, this here it is V d d and here it is 0 volt. So, what will be the condition of these two transistors? In which state they will be? What will be the mode? Will they be in off state? Will they be in linear state or will they be in saturation state? You can see here, since this is 0 here initially this is this is V d d at time t and output this V out is 0 and input is V d d. So, in this particular case this both the transistors will be on. It will be on why because this is 0 and this is V d d. So, this is acting as a source, this is acting as a source and this is acting as a drain for the p MOS transistor. So, this transistor will be on and since large voltage is applied across it, the transistor will be in the saturation mode.

Similarly, for this transistor this is this output is 0. So, this can be considered as source this can be considered as drain and this is gate. So, again this transistor will be on and since the voltage difference is v d d, again the transistors will be this transistor will be in saturation. That means, we can say both the transistors are in saturation. Both p MOS and n MOS transistors are in saturation. When when their state will change? When the condition of the transistors will change? You can see so far as the p MOS transistor is considered as 0 volt and v d d fixed. So, this transistor will always remain on. However, it may switch from saturation to linear, a a point will reach when this is equal to V t p absolute value of V t p. That means, the voltage is charging and reaches the absolute value of V t p. At that point of time the p MOS transistor will switch from saturation to linear saturation to linear mode. That means, in this case p MOS in linear. What about n MOS? N MOS case, we can see the voltage here is V d d this voltage is V d d in this particular case. What is happening? The thethe voltage the transistor is in saturation, but, what will happen? The the it will remain in saturation because the gate voltage and the gate voltage and drain voltage both are changing. We can say you can see this is this is remaining same drain drain to source this voltage is changing and gate source to both this is also changing because it is rising.

So, n MOS will remain in saturation and what about region three? Region three will occur when the voltage is at this point which is equal to V d d minus V t n. Whenever it reaches this point, then what will happen? This transistor will turn off because here it is V d d minus V t this is V d d and this is V d d. So, this transistor, the source to drain voltage will become less than V t at beyond this point. So, this n MOS transistor will turn off. That means, p MOS will continue to function in linear mode and n MOS will turn

off. So, you can see as the capacitor charges, the we have assumed that it is linearly charging. But, we shall see whether it is linearly charged or not because we can we can see here the transistor conditions are changing in the region one both are in saturation. Obviously, the current drive will be high whenever this is the case. Then as it goes to region two; p MOS is going to linear mode and n MOS remains in saturation current drive will reduce and when in the region three, p MOS in linear mode and n MOS is off. So, current drive will will be less; that means, current here we have assumed it charging at constant current. But, that is not true; that means, the current is changing as the capacitor is gradually charging. So, it will be maximum in the initial part. That this first part 0 to absolute value of V t p and in this it will be moderate and it will be low.

So, but, we have identified three regions of operation whenever you drive a large capacitive load.

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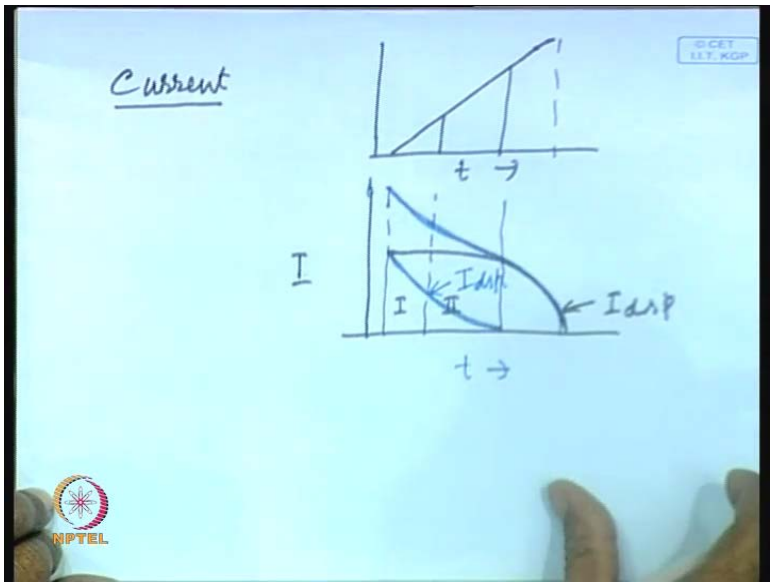

And how the current changes? Now we shall discuss how the current changes. We can we can derive the expression for current. We we have all in the last lecture we have discussed the linearly saturation current non-saturation current. I mean when the transistor is non-saturated mode, what is the expression for current and in the saturation mode? What is the expression of current that we have expressed in terms of drain voltage gate to source voltage and we know the drain voltage and gate to source voltage is various voltages are known to us because you can see here the output voltage is

changing. So, for this particular transistor the gate to source voltage is changing because it is equal to V d d minus V output. On the other hand in this case the gate voltage is remaining same; however, drain to source voltage is changing and accordingly you can derive expression for current in region one, in region two and in region three because we know the expression for current for linear and linear mode and saturation mode.

So let us consider, let me re-draw it. So, this is the time and three different regions we have already divided. Now consider the current I d i. So, let us, we have already divided into three parts starting from here. So, in the first part the the what happens to the this particular p MOS transistor? p MOS transistors is remaining in saturation in in region one and region two. In region three it is going to linear mode. So, the characteristic for the p MOS transistor will be somewhat like this. This is your V d. That means, in these in these two regions region one and region two, this is the I d s t. The p MOS transistor current is depicted by this. It it is in saturation mode in region one and region two. In the region three it is in the linear mode as we can see.

What about the n MOS transistors? For n MOS transistor we have seen it is it is in it is in saturation in region one and region two. But, in region three it is turning off, but, although this transistor is in saturation, but, its gate to source voltage is changing gate to source volt. When the when the transistor is in saturation and gate to source voltage changes, what happens? We have seen that the drain current drain current changes following square law. It is not linear at the gate voltage is reduced the. We know that I have although I have drawn it equally spaced, but, I know that we have seen that expression is dependent on V g s minus V t whole square. So, it will reduce following square law. So, that means, here what will happen? the Assuming that initially it is current is same. So, it will be somewhat like this it will reduce it will reduce not linearly, but, it will reduce quadratically. So, this is your I d s n. So, I have not really drawn I mean written the expression for currents, but, I have simply drawn the wave forms current expression you can write because you know the gate voltage you know the drain voltage and you can write the expression for drain current for p MOS transistor and n MOS transistor.

Now, the current that will be charging the capacitor, the capacitor is connected here sorry the the capacitor that will be it will be charging. Obviously, this one we will be having will the some of these currents will flow through the capacitor. So, what will be the

value? It it will be double here. So, that means, it will it will be somewhat like this. If we sum up these two this part is constant. So, it will be nature for this part nature will be somewhat similar to this because you have summing up then it will be like this. So, you can see it is not really constant. So, that means, during this period as I mentioned earlier current will be maximum in this range. But, it is reducing. Then it will it is it will first the reduce then it will become the linear mode current of the p MOS transistor. So, this will be the current that will be passing through the device. So, this is the current current that will be charging the capacitor and it will charge to 0 to V d d.

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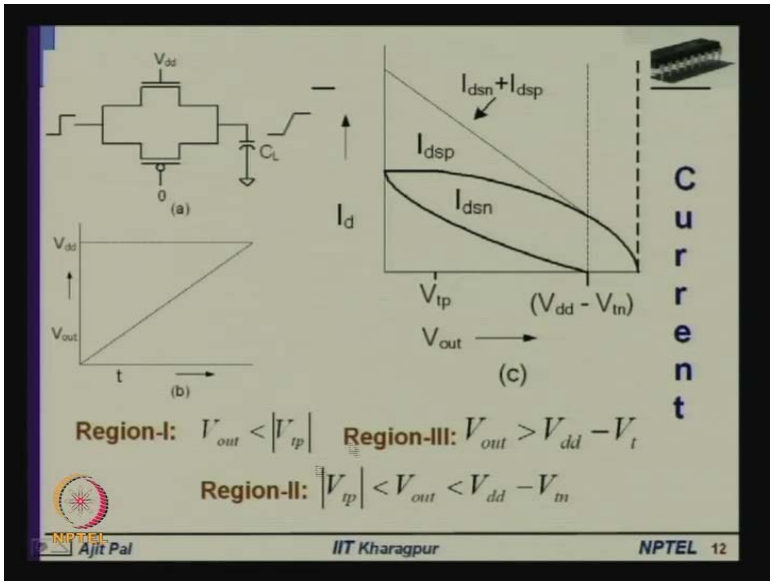

What about the yeah here the same thing is region one, region two and region three I have already explained and the the type of curve that will get I have already drawn. As you can see it is same what I have drawn on the piece of paper.

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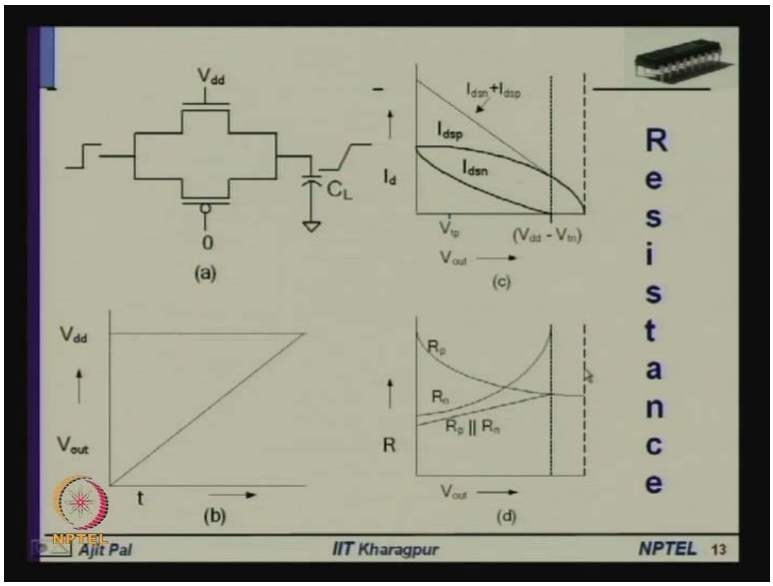

Now let us consider the resistance. So, resistance as you can see, this this is the current. How the resistance will vary? Resistance expression you can get by dividing the voltage across the devices, device by the current and you can see the n MOS transistor will turn off here. So, it is in linear mode. So, resistance is you can see gradually increasing, current is reducing resistance is increasing and it will become infinite or very high at this point when it changes switches from region two to region three. On the other hand for the p MOS transistor, it is in saturation mode. But, current will keep on decreasing because of the reduction in the value of the gate voltage. So, gate voltage is reducing. So, I mean sorry drain voltage will be reducing and the R p resistance value will be like this.

Current will remain same. Drain voltage is reducing and resistance is reducing and it will be constant because in the linear mode resistance will remain same. So, you can see we can combine these two together because they are in parallel. These two devices are in parallel. So, some of these two parallel combination of these resistors will be like this. So, you can see here, the current that will be passing through the resister is like this more or less constant.

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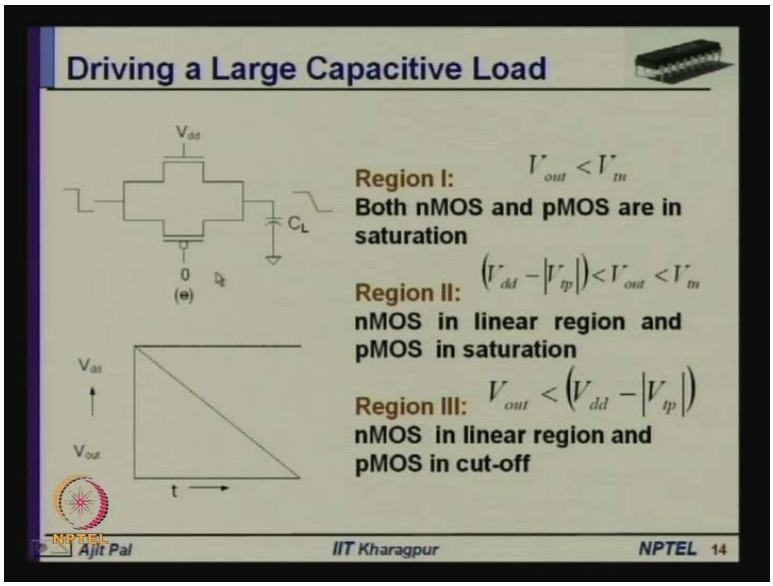

We can now consider another situation where you know the input is, earlier we have seen input is changing from low to high. Now, input is suddenly changing suddenly changed from high to low. So, in this case output will gradually discharge assuming that initially it will be high and then gradually discharge to 0. So, it will gradually reduced from 0 to V d d to 0. So, as it goes from V d d to 0 what will be the state of these three transistors? Again, you will see the operation will be, can be divided by dividing the operation I mean the entire region into three parts. In the region one, the it will be equal the V output will be equal to I mean both n MOS and p MOS transistors are on are in saturation. Initially both of them will be in saturation because you know the output here it is V d d and here it is 0.

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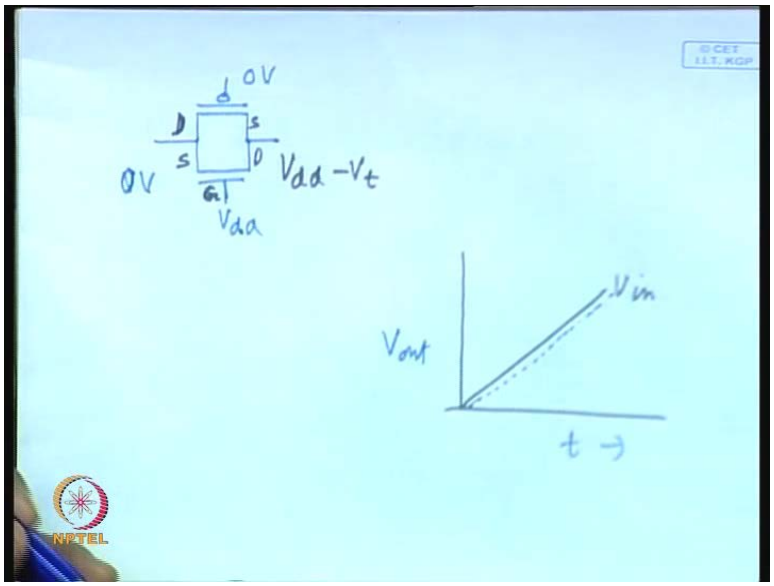

So, let me draw it so that I can explain it little better way. So, this is your p MOS transistor, this is your n MOS transistor. So, initially here it is 0 volt. You have applied 0 volt, you have applied V d d. Both the transistors are on and initially here it is V d d. Then what will be the condition? So, you can see this transistor now will be always on. n MOS transistor will be always on contrary to p MOS transistor that was always on in the previous case and this this transistor will be on also on initially because here it is V d d. So, this is the source this is the drain and this is the gate of p MOS transistor. On the other hand this is the source, this is the gate gate and this is the drain of this n MOS transistor. So, initially both are in saturation as it is written here.

But as the output voltage, so, this is connected to V d d and this is connected to 0. So, as the voltage reduces to V d d minus V t, then this transistor switches from saturation to linear mode. Of course, this transistor remains in saturation. So, because you know that gate gate to source voltage and drain to source voltage is you know, the difference is now V d d minus V t. So, this this goes to saturation to linear mode as it is written here n MOS in linear region and p MOS in saturation region when the output voltage is going from V d d to minus V t p. And finally, in the region three when the output is V d d minus V t p n MOS in linear region, it remains in linear region and p MOS in cut-off region.

So, you can see the p MOS continues to operate, continues to remain on, but, p MOS transistor turns off. So, as it is shown in this diagram, this is how it happens. Region one v output is less than V t n. So, n MOS transistors remains in saturation for both region one and region two. But, the p MOS transistor turns off here and at this point when the output is V d d minus V t p and so we can see the the operation is somewhat similar. But, the role of the p MOS and n MOS transistor changes in this particular case and accordingly we have just like the previous case, current current is drawn. This is this is the p MOS transistor current. This is the n MOS transistor current and these are some of the two currents and similarly, the resistance also will be somewhat similar only difference is the role of n MOS and p MOS transistors. As you can see the resistance is somewhat identical to the previous case.

Now, let us consider another very interesting case when the output is a small capacitance. You have connected a small capacitance to the output of the transmission gate. So, whenever the output capacitance is small what will happen? As the input changes from 0 to V d d; since the capacitance is small it will charge very quickly. So, if it is charged slowly then, the output will follow the input with small difference. That means, if the in this particular case if this is the input; if if this is V in output will be this is time and this is V output. So, this it will be somewhat like this. That means, the output will follow the curve, follow the input voltage, but, with the difference.

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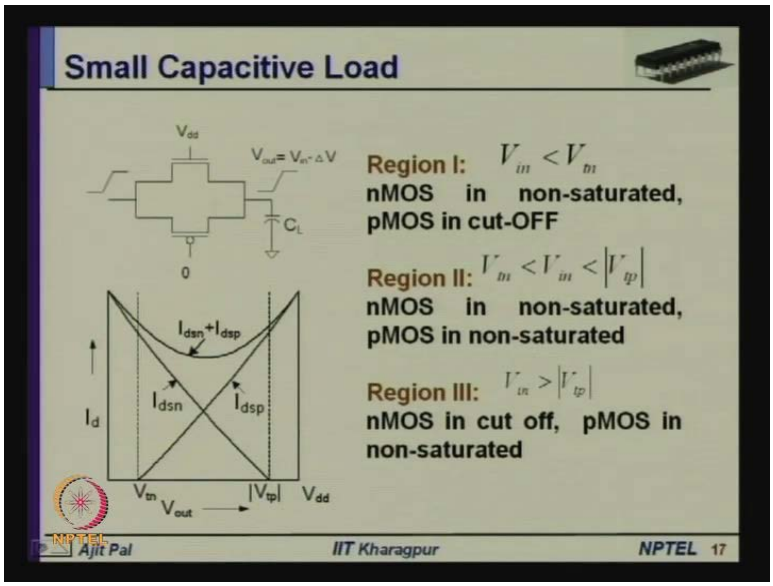

And in this particular case again you can divide the operation into three regions as the input changes from 0 to V d d. Region one; V in is less than V t n. n MOS in non-saturated p MOS in cut-off. One interesting point is here, you can see voltage difference is always very small between the input and output. And as a consequence the transistors will never be in saturation mode because you require a high voltage across it for the transistors to remain in saturation mode. That is why initially n MOS in non-saturated, p MOS is cut-off the. Then as you go to region two then n MOS in non-saturated and p MOS is non-saturated and as you go to region three n MOS is cut-off and p MOS in non-saturated as it is shown here.

So, V t n to V t p absolute value of V d d actual be actual it will be V t p and this is your V d d. So, you can see here, the current for the two transistors are shown here for the n MOS transistor current reduces quadratically. Here it is shown I mean linear curve, but, it will be a quadratic line. So, it will it will reduce quadratically for n MOS, p MOS transistor the current will pick up quadratically up to this region. So, it will turn on here initially we have seen it was off. So, in the first part it was off then it will build up quadratically because the gate voltage is increasing. On the other hand for n MOS transistor it will decrease quadratically because gate voltage is reducing gradually, because input is linearly increasing. So, this will be the current that will be passing.

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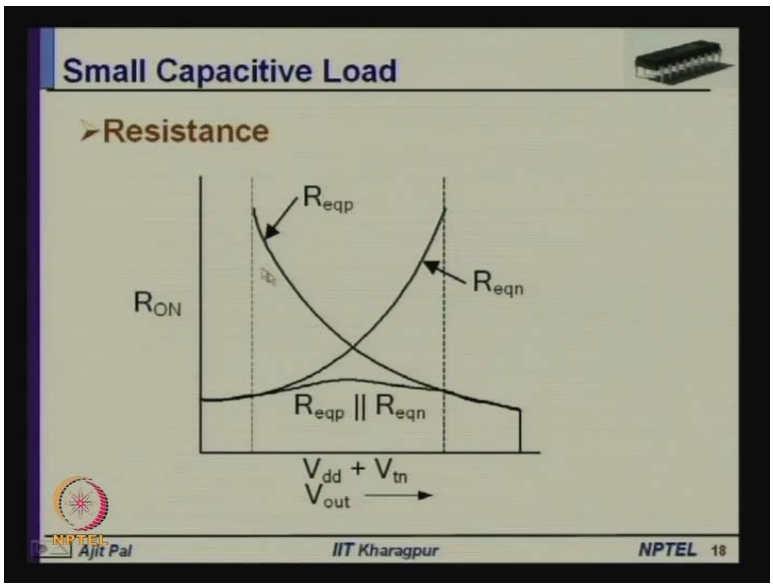

Similarly, I can find out the equivalent resistances. This is the resistance of the p MOS transistor. Initially it will be very high because it was off in this region. Then it is it will reduce gradually for n MOS transistors initially it will be low, then it will increase and it will become very high or infinite as it reaches goes from region two to region three and the current will be the parallel value of resistance is more or less same as you can see it remains constant.

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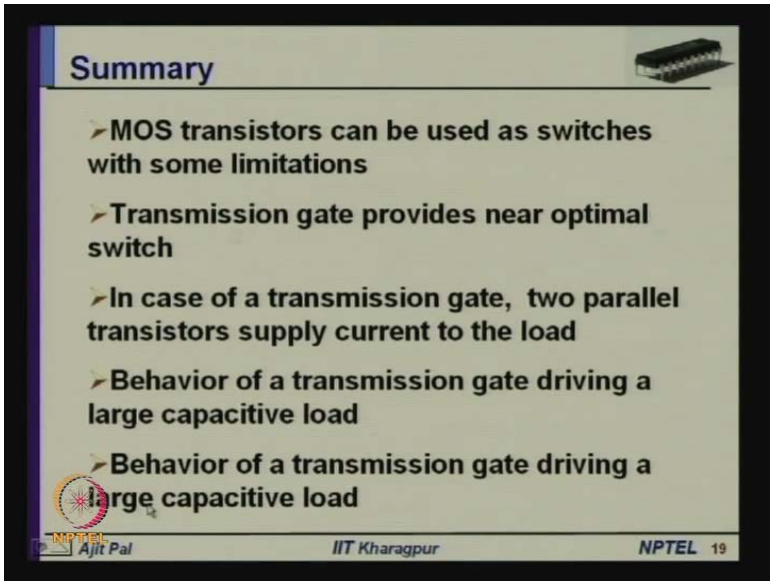

So, we can summarize what we have discussed today. We have we have seen MOS transistors can be used as switches of course, with some limitations and transmission gate provides near optimal switch as you have seen it is close to closer to ideal. Then we have seen in case of transmission gate to parallel transistors supply current to the load and behaviour of transmission gate driving a large capacitive load has been discussed in detail. Behaviour of a transmission gate driving a small capacitive load, it will be small. Here is a typo of small capacitive load has been discussed in detail. So, with this we have come to the end of today's lecture and our discussion on MOS transistors. And as we are following the bottom up approach, in the next class we shall discuss the operation of MOS inverters.

So, we shall start discussing on MOS inverters starting from next class. Thank you.