Low Power VLSI Circuits and Systems

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Lecture No. # 04

MOS Transistors – III

Hello and welcome to today's lecture on MOS transistors. This is the fourth lecture on the low power VLSI circuits and systems course and third lecture on MOS transistors. In the last lecture we have discussed how the operation of a MOS transistor can be visualized with the help of a very interesting model known as fluid model and fluid model as we have seen can be applied to charge controlled devices including MOS transistors. There we have seen how the MOS transistor operates and how the the current flow through the channel between the source and drain can be controlled with the help of gate voltage and also the drain voltage. And we have seen that there are three modes of operation.

One is the accumulation mode, another is the linear mode and third one is the saturation mode. And based on that the characteristic of MOS transistors can be divided into three regions as you have seen cut-off cut-off region, linear region, linear or active or you know that that partially charge controlled device. That means, partially that that is actually called when the inversion region is partial, weak inversion region and then the strong inversion region is represented by saturation region rather weak strong inversion mode is represented by saturation region.

And today I shall discuss the electrical characteristics of MOS transistors.

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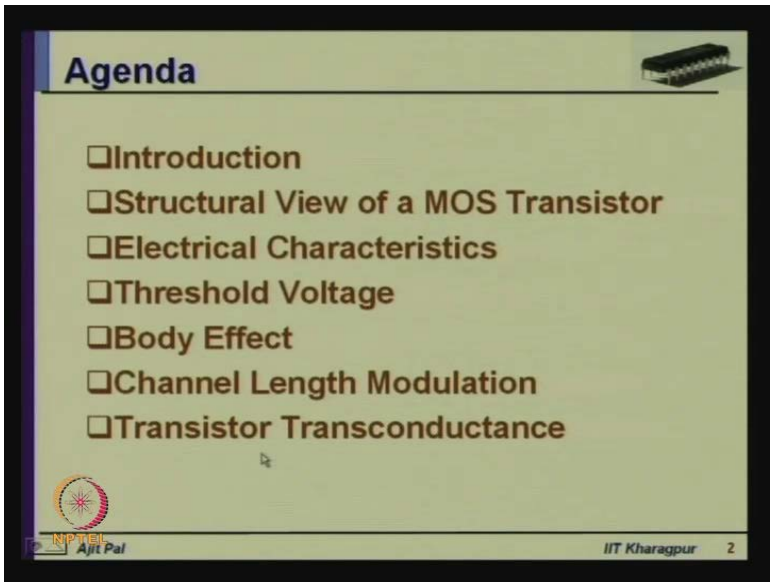

And here is the agenda of today's lecture after a brief introduction I shall I shall show once again the structural view of a MOS transistor and which I shall use to explain the operation and also derive expression for MOS, the the the drain current and particularly which is known as the electrical characteristics of MOS transistor.

Then, I shall discuss some about some of the important parameters like threshold voltage and another related subject related topic is body effect and we shall see how this how the substrate voltage can be changed to change the threshold voltage with the help of body effect. Then, another important phenomenon is known as channel length modulation I shall discuss about that and finally, I shall discuss about transistor trans-conductance.

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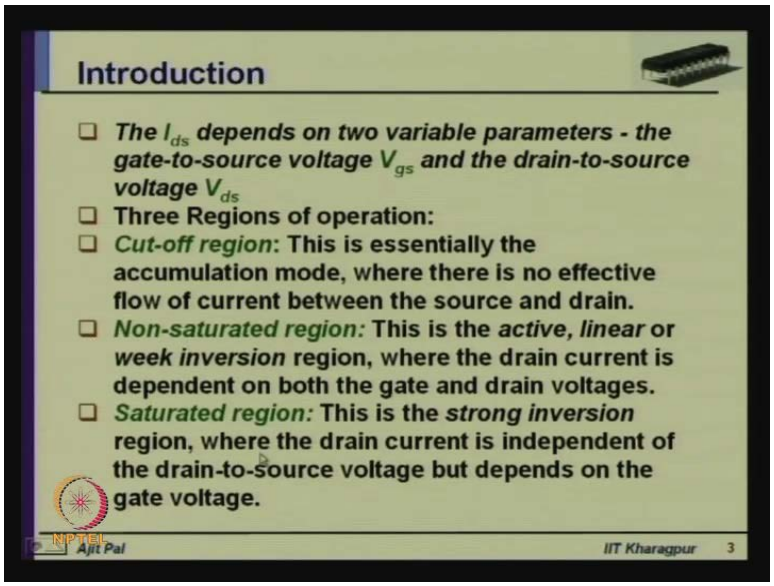

So, here is the introduction as I have already mentioned the drain current IDS depends on two variable parameters; the gate-to-source voltage V g s and drain-to-source voltage. Of course, here I did not mention about another important electrical parameter. That is your body bias that is your body-to-drain body-to-source voltage rather source-to-body voltage. That also affects the operation and with the help of which the threshold voltage can be controlled. So, essentially three voltages; gate-to-source voltage, drain-to-source voltage and the source-to-body voltage. These three voltages will control the drain current.

And as I have already mentioned there are three regions of operation; the cut-off region and this is represented by the accumulation mode where there is no effective flow of current between the source or drain source and drain. And we have already seen in this mode actually gate voltage is less than the threshold voltage and there is no channel formation. So, there is no inversion layer. So, there is no channel through which current can flow. So, in this particular region there is no flow of current, no effective flow of current between the source and drain.

Here I am telling effective flow. The reason for that is there is very small amount of current that flows through the device. But, for all practical purposes we can neglect it. That is why we are calling it effective flow of current I mean the no effective flow of

current. But, very small amount of current flows as we shall see that is represented by the sub-threshold leakage current. Later on we shall discuss about it in more detail.

Then, we shall consider the non-saturated region. This is the so-called active linear or weak inversion region as I have mentioned and here the drain current is dependent on both the gate voltage and drain voltages. So, the the as we shall see the expression for drain current will be dependent on both gate and drain voltages. Then the third region which is represented by the saturation region; this is the so-called strong inversion region where the drain current is dependent on the drain-to-source voltage. But, depends, but, does not depend on the here there is a mistake does not depend on the gate voltage sorry there is it does it is independent of the drain-to-source voltage, but, depends on the gate voltage. That means, in the saturation region the drain current solely depends on the gate voltage. It does not depend as we change the drain voltage as we shall see.

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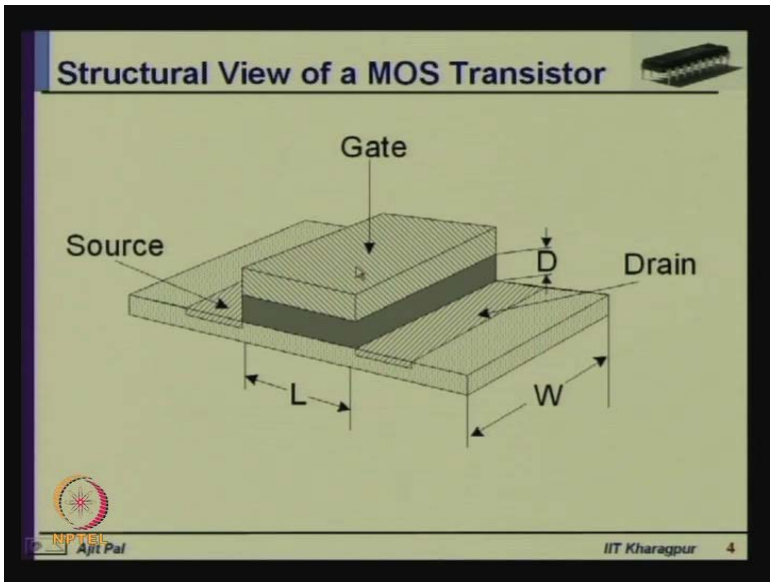

So, these are the three different regions. Now, I have already shown you this structural view in the last lecture and particularly there are three important physical parameters. I am calling it physical because when you do when you do the fabrication of a MOS transistor then you youyouyou will decide the length of the channel, the width of the channel and thickness of the silicon dioxide. These three are decided at the time of fabrication. So, these physical parameters will affect the operation of a MOS transistor and obviously, the electrical characteristics of the MOS transistor. So, we shall express

the drain current in terms of these three physical parameters L which is the length of the channel, W the width of the channel and D thickness of the silicon dioxide layer.

And as you can see on both sides of this channel we have got the source. I mean the the the the diffusion regions, heavily diffusion regions and here also we have got another diffusion region that is called as drain. So, you have got source and drain and here is the gate on top of the silicon dioxide. We put polysilicon layer to form the gate and we can take electrical connections from source gate and drain to realize circuits. Later on we shall discuss about that.

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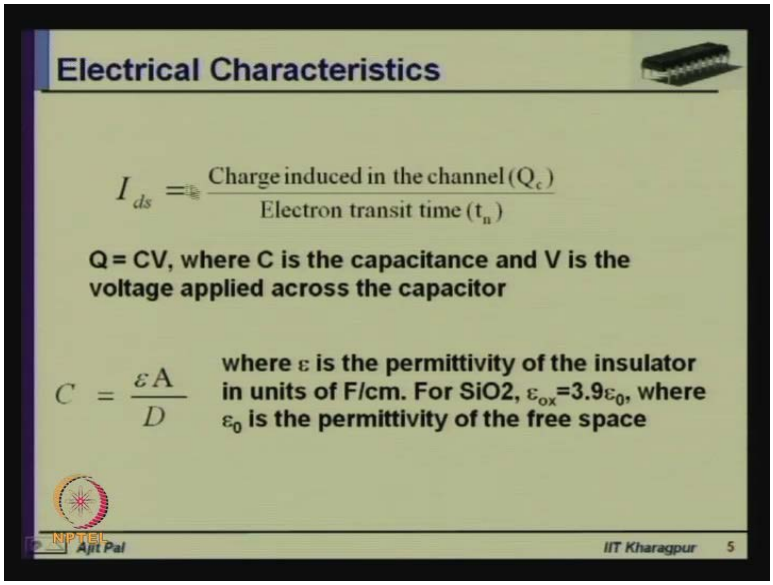

Coming to the electrical characteristics; I shall try to derive the expression for drain current in the same line of the fluid model. We have seen in the fluid model because of the voltage that we applied at the gate some charge is induced. So, inversion layer is created. Charge of opposite polarity in case of n MOS transistors it is the it is the electrons which are created and that charge can flow. Rather current can flow between source and drain whenever you apply some voltage between source and drain.

So, charge is I mean that in weak, in the inversion region is created because of the gate voltage that we apply. And then because of that creation of charge a conducting path is obtained which is known as channel between the source and drain and current will flow when you apply a voltage, you apply an electric field between the source and drain by applying a voltage to the drain with respect to the source.

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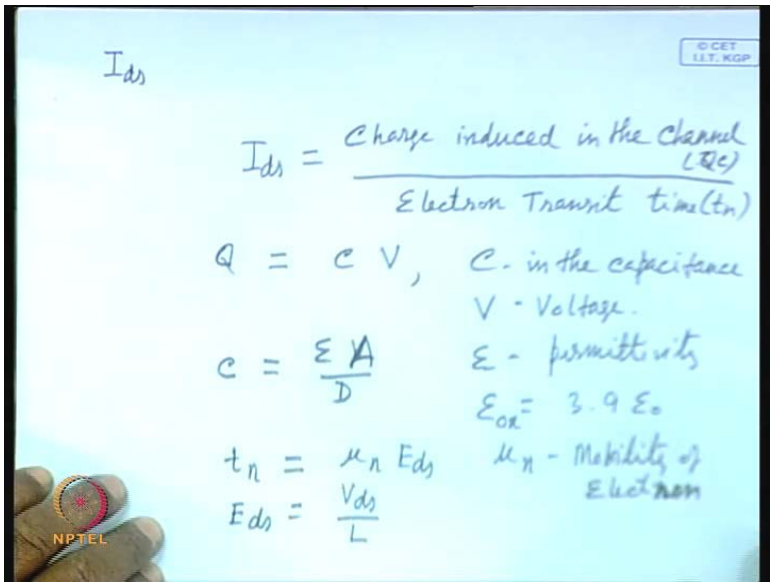

So, let me write down the drain current expression. So, Ids drain-to-source current. So, Id s can be represented as charge induced in the channel charge induced in the channel which you can call at I c rather Q c and that can be divided by the electron transit time electron transit time transit time is t n. So, that means, here as you can see not only creation of charge is important or formation of inversion layer is is important; it is necessary that the electron will move from source to drain as we apply a voltage electron will from from one end source end to the drain end and that will lead to a constant flow of current and as a consequence this electron transit time is important. So, as you know that Q that charge that is accumulated in a parallel plate capacitor is equal to c into V where C is the capacitance C is the capacitance and as you have seen it can be consider as a parallel plate capacitor and V is the voltage that is applied across the parallel plate capacitor.

And as you know this capacitance C is equal to epsilon V epsilon a, area of the plate and the D thickness of the silicon dioxide layer. So, here epsilon is the permittivity of the insulator permittivity permittivity of the insulator and this e will be equal to you know in this case we shall be using silicon dioxide. So, epsilon o x is equal to three point roughly approximately 3.9 epsilon 0 where epsilon 0 is the permittivity of the free space and this we shall use to represent the, to to find out the expression for the current.

Now, this is the expression for capacitance. What about the electron transit time? T n t n will dependent on what what thing? First of all it will depend on two things; number one is speed and second thing is the distance. So, you can say that transit time t n will be equal to mu n into E d s. That means, mu n is the mobility of electron mobility of electron. Here we are considering n MOS type transistor. So, the charge carrier are electrons. That is why we are considering mobility of electron and E d s is the, is a drain-to-source electric field. We shall find out what is the drain-to-source electric field E d s it is dependent on what? It is dependent on the voltage that we apply across the across the drain-to-source. So, the E d s will be equal to V d s by length l. So, E d s by l.

Now, based on this we can find out the the electron transition time. So, electron transition time will be equal to.

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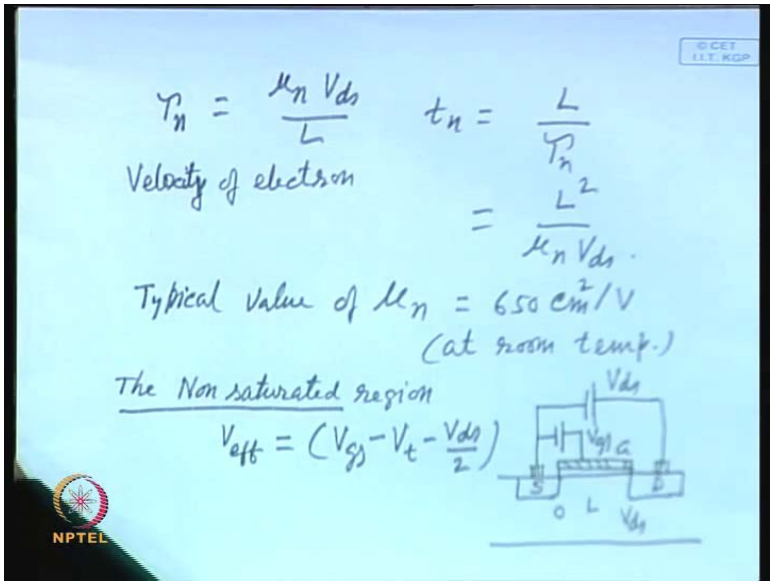

First of all let us find out the velocity of electron tau n. Tau n is equal to mu n V d s by l and therefore, t n electron transition time, this is the velocity of electron and t n will be equal to electron transition time that will be equal to l by tau n, length by tau n that will be equal to l square mu n by V d s. So, we have got the the expression for the electron transition time and and it has been found that typical value typical value of mu n mu n that is the mobility of electron is equal to 650 centimeter square by volt and that is at room temperature.

So, we have got the expression, we have got the the value the the charge that we can obtain by C into V and we can we have, also found out the electron transition time t. Now, we can find out the current I d s now to do that we shall divide the entire region into three parts as we have seen. Number one is cut-off region when the voltage is less than the threshold voltage, there is no channel formation. So, there is no current. So, we are not writing any expression for current for that.

Now, we shall write down the expression for the non-saturated region. Non-saturated or we also call it linear or weak inversion region. In this weak inversion region, we can find out the the the the current. First of all let us find out the effective voltage that is being applied between the source and drain. As you have seen, we are applying a voltage V d s between the source and drain sorry on the gate I mean V d s between the source and drain. Let me draw the diagram here little that will make it easier to understand. So, here is your source and here is your drain. This is the channel then you have got the silicon dioxide and top of that you have polysilicon.

So, what you are doing? You are applying a voltage V d s, positive voltage. So, this is your V d s between the source and drain and you are all supplying a voltage V g s between source and gate. This is your source drain and this is your gate. So, V g s, now although you are applying a voltage V g s between the source and gate; the effective voltage across the channel is not same because this drain voltage that you are applying is interacting with the voltage that you apply at the gate. So, although you are applying a gate voltage V g s here, the effective the effective voltage in this channel region will be different.

For example in here the voltage you know that the the the the voltage V d s will be will will be across this length L and here you can say the voltage is 0 and here the voltage is V d s. So, if you take the average value of 0 and V d s this will be equal to V d s by 2. Therefore, the effective gate voltage will be equal to V g s that you apply here minus V t threshold voltage as we know, you the you have to subtract that threshold voltage because you know the before that there will be depletion region. You will you will require a voltage V t only after that the inversion region starts and as a consequence the effective gate voltage will be V g s minus V t minus V d s by 2. We have taken the average value. Of course, it will be it will be varying across the channel, but, we are taking the average value. This is the effective gate voltage.

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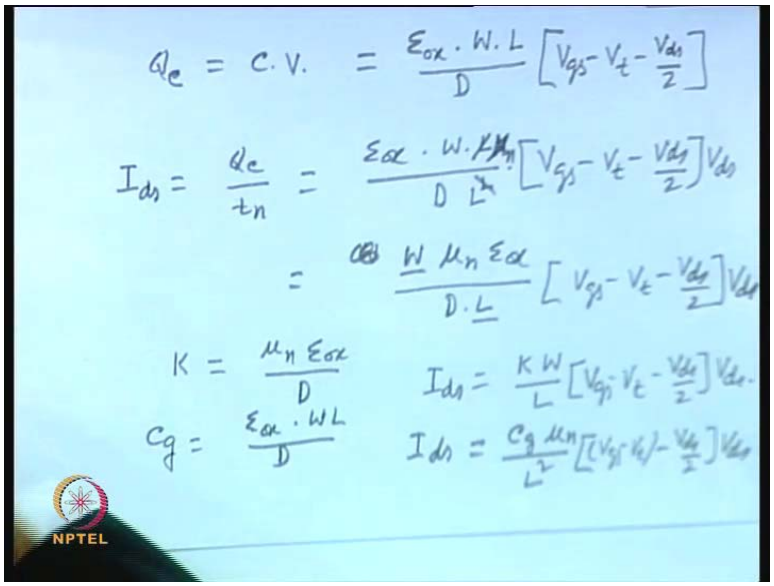

Now, the current, we can derive the expression for current we can expression for current. For that purpose first we shall find out the Q c. This Q c charge induced in the channel is equal to C into V. That means, C is equal the Q c is equal to C into V that is equal to C. What is C value of C? Epsilon, this is your oxide into into area that is equal to W into L because we have seen that parallel plate capacitor has an area W width W and L is the length. So, area is equal to W into L by D. This is the this is the capacitance and your effective voltage will be equal to V g s minus V t minus V d s by 2. So, this is the this is this is a charge that will be induced in the channel.

So, this is the charge and now we know the we already know the electron transit time. What was the electron transit time that you find out? This is equal to L square by mu v d s. So, this we can substitute. That means, I d s I d s is equal to Q c by t n that is equal to epsilon oxide into W into L by D into V g s minus V t minus V d s by 2 and it will be divided by L square. This is the expression for electron transit time. This is the L square t n is equal to L square by mu n d V s.

So, what will happen; here you will have L square and mu will be here, mu n will be here in the numerator it will go to the numerator and here you will have V d s. So, this is the this is the expression that we get. This is mu n and this l will cancel with square. So, ultimately we get an expression that is equal to W L. It was L square W L by d, the current expression that we get is equal to W mu n. This is mu n epsilon o x. This is your

permittivity of electron into D into L and here you get V g s minus V t minus V d s by 2 into V d s. Now, this is the this is the this is the current that flows through the electron. So, that will be the current that will be flowing through the electron.

Now, you can express in terms of two other important parameters; one is known as K. K is a constant which depends on the fabrication. So, what is the value of K? K is equal to we can express it this current in terms of K which is equal to mu n. This mu n and epsilon o x by D. You know when you fabricate; these three parameters are kept usually constant. We usually change the length, this L is changed, width is changed, but, these three are usually kept constant. That is why this is sometimes is replaced by K. That means, if we substitute this value of K we get I d s is equal to K W by L V g s minus V t minus V d s by 2 into V d s.

Another we can also represent it in terms of what is known as the gate capacitance C g. What is the value of C g? C g is equal to this is your e o x into W L by D. That you have already seen that is a capacitance. This this is the, you have already seen epsilon A by D here a is equal to W by L. So, we can also express I d s in terms of this capacitance. So, in terms of K constant in terms of C g. So, I d s we can write as I d s is equal to C g mu n by L square into V g s minus V t minus V d s by 2 into V d s . So, this is the current that we get whenever the circuit is in the linear region.

It may, you may note that we are calling it linear region, but, it is not exactly linear. Why it is not exactly linear because you can see, if we assume that V d s by 2 is too small compared to V g s minus V t. Only then it becomes proportional to V d s. That means, if we neglect this part only then it becomes linear and that is a reason why the this the linear region is not exactly linear, but, it approximately linear, particularly when the drain voltage is very close to 0. Only then it is linear so; that means, V d s is negligible compared to V g s minus V t then is linear.

So, we have derived expression for the non-linear region.

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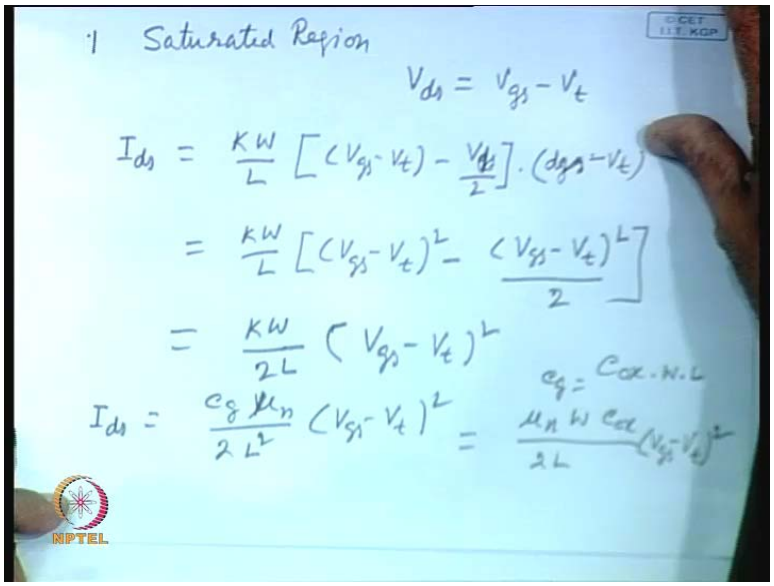

Now, let us consider the saturated region. So, you can say the second part is your saturated region. So, in the saturated region what is the K difference between the linear region and saturated region? One important difference is in the saturated region, the current is independent of the drain voltage and when it happens? When the voltage drop across the channel is equal to the effective gate voltage. That mean if the drain voltage is such which is equal to V d s is equal to V g s minus V t. That means, this occurs when V d s is equal to V g s minus V t. This is the effective gate voltage which is equal to the drain voltage beyond which, beyond this point the drain current is independent of V d s. That means, this is the point from where we can consider we can say that saturated region has started below that it is linear or non-saturated region.

So, what we can do, we can obtain the expression for drain current in the saturated region by substituting V d s is equal to V g s minus V t. So, we can say that I d s is equal to K W by L into V g s minus V t minus V g s by 2 into here you can substitute this. sorry This is d s V d s minus sorry V g s minus V t. We are substituting this V g s minus V t. So, this is equal to K W by L into V g s minus V t square and here it becomes, here also it will be V g s minus V t. So, it will be equal to V g s minus V t square by 2.

So, this will be equal to K W L by 2 because half this if we V g s minus V t square minus V g s minus V t square by 2 will become V g s minus V t square by 2. So, this will be equal, this two we have taken here. So, K W L K W by 2 L into V g s minus V t square.

So, here indeed we find an expression where it is independent of the drain voltage. So, but, it is there is a it is a there is a square law dependence on V g s minus V t. That means, this saturation current will increase at the square law as the gate voltage is increased. So, that is proportional to V g s minus V t square. So, this is the expression for drain current and also you can express it in terms of the capacitance that will be equal to C g mu n by 2 L square into V g s minus V t square.

So, this is the expression for that. That in terms of C g gate capacitance and of course, you can you can represent it with the help of another parameter. There is another parameter which is known as C o x C o x and C g these two are different this C o x is the unit gate capacitance. That means, capacitance of unit area. So, what is a relationship between C g and C o x? C g will be equal to C o x into W that area you have to multiply W into L. So, C o x into W into L if we substitute it here. We can write it in this way, this l it will become it l square this l will cancel out. So, it will be mu n will be there in any case then w will be there and it will be C o x by 2 into L and here it will be V g s minus V t square. So, this is in terms of the unit gate capacitance C o x.

So, we have seen the expression for saturation current.

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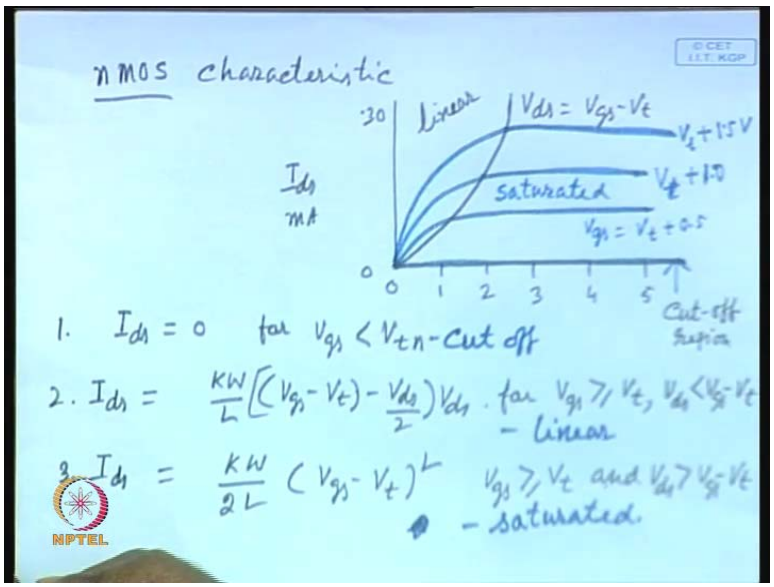

Now, let us represent the n MOS electrical characteristics n MOS characteristics. Let us now plot that saturation and non-saturation current. We have seen that we can divide into three regions. Let us assume it varies from 1 2 3 4 5; 1 volt 2 volt 3 volt 4 volt and 5 volt

and this I d s usually varies in the range of in the milliampere region. So, it is milliampere. So, 0 to let us assume it is 0.30 milliampere. So, usually it will vary in this region.

Now, as you have seen there are three regions; I d s is equal to 0 for V g s less than V t. We can write V t n if we consider it n MOS transistor. So, which part will represent that? This line, that means, this line will correspond to this particular line will correspond to this region. That means, irrespective of the drain voltage current is 0, I d s is 0. So, this represents the cut-off region cut-off region. So, this this is your cut-off region.

Now, non-linear, linear region I d s is equal to we have already seen the expression. We can write it K W by L into V g s minus V t minus V g s V d s by 2 into V d s. This part as we have seen is separated by a line. I mean this corresponds to V d s is equal to V g s minus V t. That means this part is your linear region. So, obviously, there will be different curves for different gate voltages.

Say this is this corresponds to V. Let us assume V g s is equal to V t plus 0.5 volt. Let us assume this corresponds to V t plus 1 volt 1.0 volt. This will correspond to let us assume this is V t plus 1.5 volt. So, the in this part the current is constant this part current is constant. So, this is a saturation region. So, this is the linear region, this is the cut-off region and this is the saturation region saturated region and in the saturated region the current expression is given by and this is for this non-saturated region is for V g s is greater than equal to V t and V d s is less than V g s minus V t. That means, V d s has to be less than V g s minus V t in this region and V g s has to be greater than V t.

So, for these two we call it linear region. This is cut-off this is your cut-off region cut-off. This corresponds to cut-off region. This corresponds to linear non-saturated or weak inversion region and this correspond the third region this is your 1 2 and 3 I d s is equal to, we have seen the expression is K W by 2 L into V g s minus V t square and this happens when V g s is greater than equal to V t and also V d s has to be greater than V g s minus V t. So, this is your saturated region. This corresponds to saturated.

So, we have seen, we have derived the expression for drain current for two regions; linear and saturated regions and we have defined the regions based on the drain voltage and gate voltage. Here, we have not taken into account the body voltage with respect to the source. We have assumed that the body is connected to the source.

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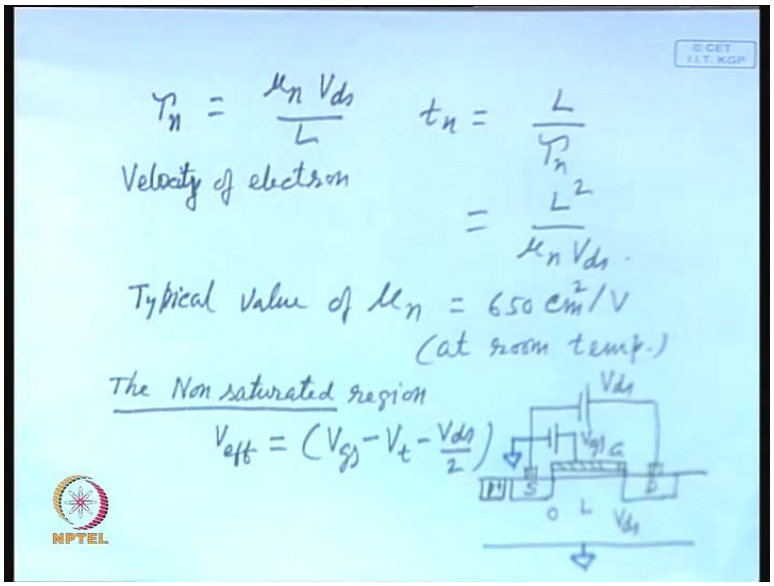

That means, if we consider this diagram, this simple diagram we can say this body is connected to ground. That means, this is connected to ground. Source is connected to ground and body is also connected to ground and usually this is done you know by having a region, this is called P plus and this P plus is actually used to connect the substrate to ground or to some other voltage. Later on we shall see how we can really apply this voltage to have different threshold voltages. So, for the time being let us assume that this drain, that source to substrate voltage is 0.

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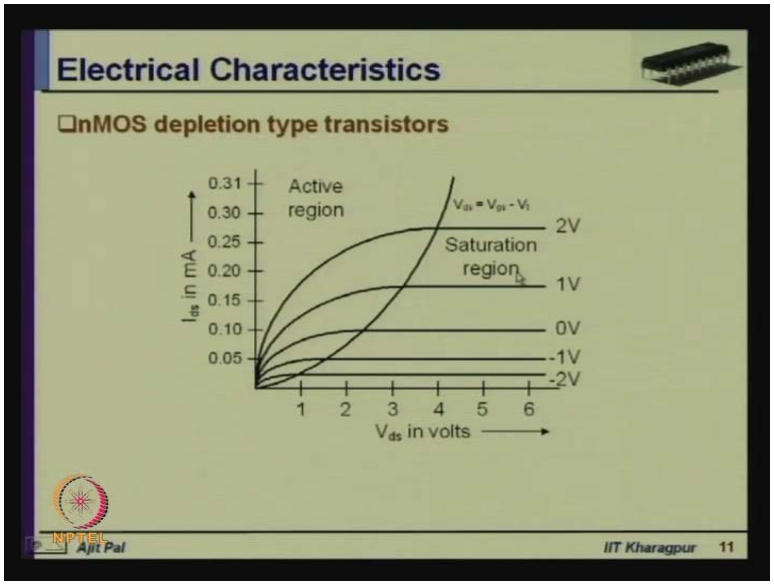

Now, we have considered the n MOS depletion type, we have n enhancement type transistor. Let us now focus on n MOS depletion type transistor and as we know in case of n MOS depletion type transistor, a channel formation is done by implanting suitable type impurity in the channel region. So, a conducting layer already exists and as a result you do not require a gate voltage to to form a channel. So, current can flow even when the gate voltage is 0 and you can you can stop the flow of current by applying a negative gate voltage and that is precisely shown in this diagram. You can see here even when the gate voltage is 0; there is a flow of current and if you want to stop it you have to apply negative voltage. That means, minus minus minus 1 volt minus 2 volt and so on.

Otherwise, there is no difference in the characteristic curve. I mean it is very similar to the n MOS depletion type. I mean enhancement type transistor except that these gate voltages are different for different currents. That means, normally in case of enhancement type transistor this will start when the gate voltage is slightly more than the threshold voltage. But, here as you can see this is minus 2 volt. So, in case of depletion mode of transistors only difference that we will get is the for different gate voltages you will get different curves. That means, you have to apply a negative voltage to stop the flow of current and if you apply positive gate voltage then current will increase and obviously, as we know that it will increase following square law V g s minus V t square.

So, we have seen the characteristic curve for n MOS type transistors both enhancement type and depletion type. What about the P type transistors?

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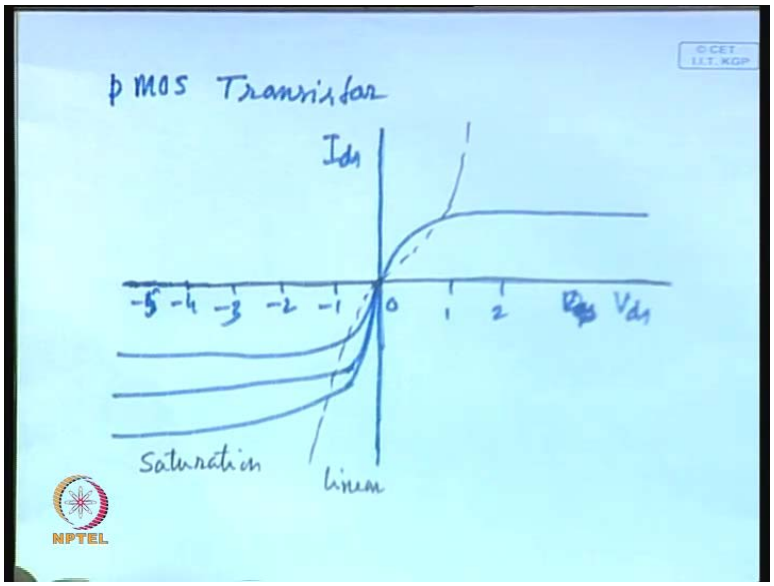

Actually that can be drawn say P MOS transistors. We shall not derive expression for that I shall simply show you the characteristic curve, how it will look like. So, you have got four quadrants. You can see here, you have got four quadrants. This is your I d s and this is your V g s. This is positive and this is negative. For n MOS transistors, the curve is on this side. On the other hand for P MOS transistors the curve will be on the negative side. That means, you will be applying your the voltage, that drain voltage sorry this is your V d s. I have written wrongly V d s. So, here it will be negative here also V d s, but, here it is say 0 1 2 here it is minus 1 minus 2 minus 3 minus 4 minus 5 and so on

That means you will apply negative gate, negative voltage to the drain with respect to source and current will flow in the opposite directions. And these are for different different gate voltages and more negative they correspond to more negative gate voltages. And just like your n MOS transistors here also, there is a there are three regions cut-off. So, just like your n MOS n MOS transistor here also, you have got linear region, this is a saturation region and this line obviously, will represent the cut-off region. This is a cut-off region for p MOS transistor, this is a cut-off region for n MOS transistor. So, on; that means, this this this the the characteristic curve for p MOS transistor will be on this quadrant both for enhancement type and depletion type.

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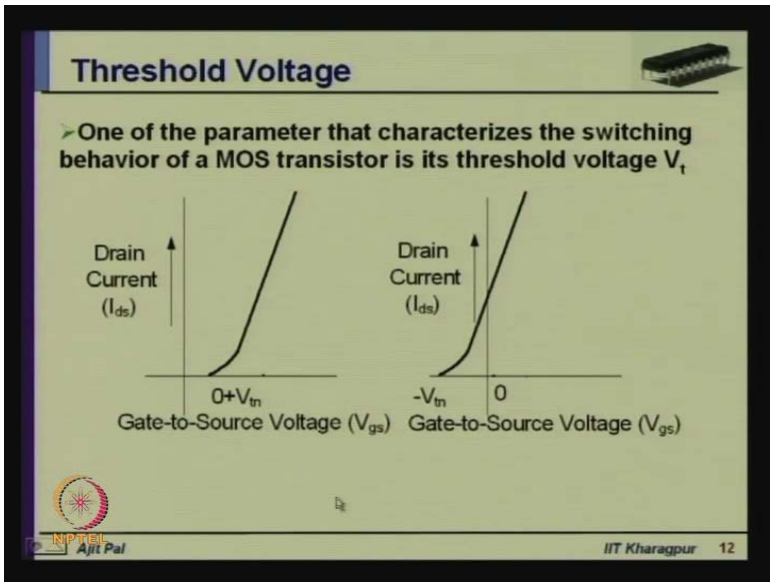

Now, let us focus on the threshold voltage. This threshold voltage has been found to be one of one of the most crucial parameter which controls the operation of a MOS transistors MOS transistor. So, here you can see this corresponds to n MOS enhancement type transistor. You have to apply a threshold voltage I mean V t n to start the flow of current and characteristic curve will be somewhat like this. That this is the drain current will increase and as you know this essentially represents the the the the drain current in the saturation mode. That means, in the saturation mode, although I have drawn it linearly, but, it will be quadratic. As we have seen this current is proportional to I d s is proportional to V g s minus V t square. So, it increases at this rate.

So, far as the depletion type transistor is concerned; curve is somewhat similar, but, it will be shifted towards the towards the negative quadrant. As you can see you have to apply a minus V t n, a threshold voltage which is the minus V t n in this case to stop the flow of current and if you increase the the I mean negative to less negative to 0 and then positive; then the drain current increases following the same nature of curve and of course, the the amount of current will be dependent on the gate voltage. So, you can see the the thethe these two essentially represent the the drain current with respect to gate-to-source voltage for enhancement type transistor and for depletion type transistor.

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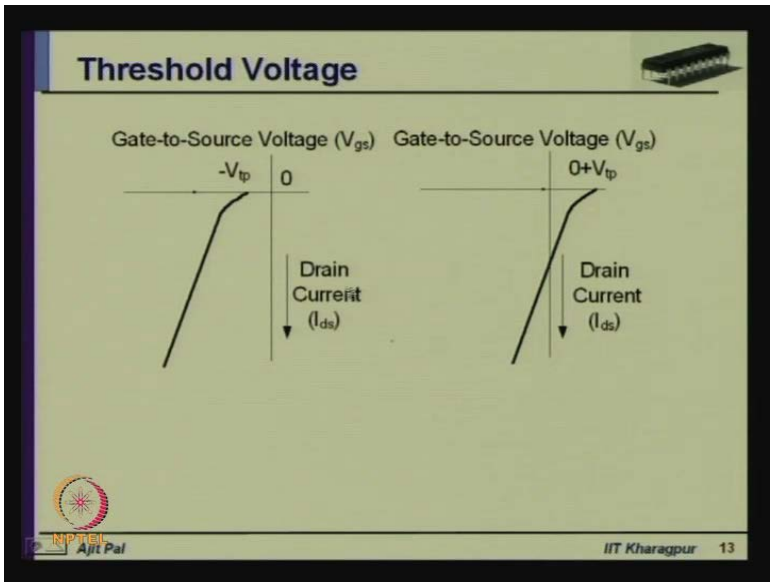

Similarly, you can consider the gate-to-source voltage for p MOS type transistors. This corresponds to the characteristic curve for p MOS type transistor. Here you can see the variation of drain current with respect to the gate volt gate-to-source voltage. And a negative voltage is required to for the flow of current and you can see the curve is somewhat similar, but, inverted in this case because in the it is in the negative quadrant. Similarly, this is this this curve correspond to corresponds to the p MOS depletion type transistor and here as you can see you have to apply a positive voltage to stop the flow of current and as you as you make it smaller and smaller and when it becomes 0; this side is the gate-to-source voltage. So, when it becomes 0 still there is a flow of current and as you make it more and more negative; the current increases in case of p MOS depletion type transistor.

So, these four; these two and these two represent the the variation of gate drain current with respect to the variation of gate-to-source voltage and you can see the threshold voltage actually plays plays acts somewhat like the cutting voltage of you know cutting voltage of bipolar junction transistors. As you know in case of bipolar junction transistors flow of current is dependent you know, you require a cutting voltage. For example, for silicon the base base voltage should be more than 0.6 or 0.7 volt. That is known as cutting voltage. Here also here also it is somewhat similar to that, but, we call it threshold voltage not cutting voltage.

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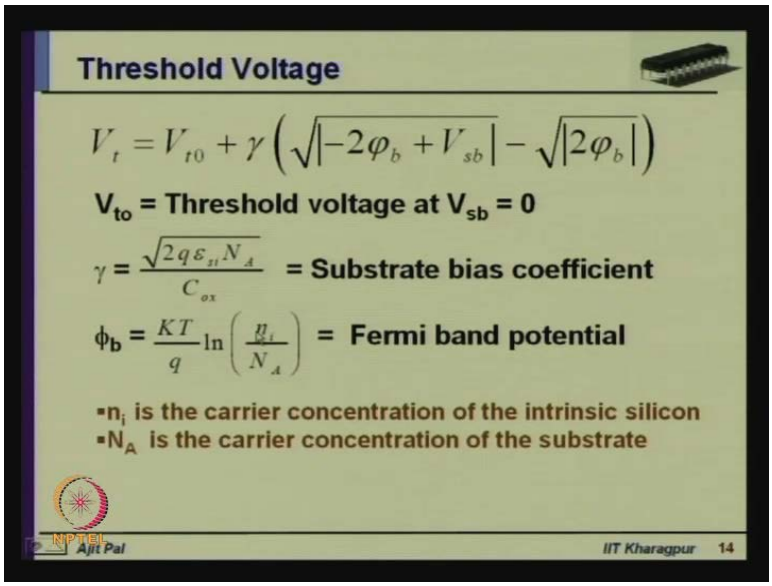

Now, one one very important as I told threshold voltage plays a very important role and on what factors or parameter it depends? You can really derive an expression for threshold voltage in terms of various parameters, but, here I have simply taken the expression without and I am not going to derive it and as you can see V t, the threshold voltage is equal to V t 0 plus gamma into root 2 phi minus 2 phi plus V t V s b absolute value of that and minus absolute value of 2 phi b.

Here this gamma is known as substrate bias coefficient. Why substrate bias coefficient? As you can see this V s b V s b is actually the source-to-body voltage that you are applying source-to-body voltage that you'll be applying. That means, if we consider a a curve here you can apply a voltage between the source and body. That means, the this particular source and this body you can apply positive voltage to the body with respect to the source and that will actually increase the threshold voltage as we shall see.

So, by changing the body bias, substrate body bias the threshold voltage can be controlled and in this expression you have got V s b. That is why it is called substrate bias coefficient gamma. And gamma is equal to root 2 q. Q is the charge of electron epsilon s I which is the permittivity of electron and n a n a is the carrier concentration in the in the in the substrate. So, n a is the carrier concentration of the substrate and C o x C o x is the unit unit capacitance of the gate region.

So, this is the expression for gamma. So, it will depend on these parameters and phi b is the fermi band potential which is equal to K t by q. K is the Kelvin constant and t is the temperature in absolute value of temperature not in degree or Fahrenheit this is the absolute value of temperature and Q is the charge of electron and n i is the carrier concentration of the intrinsic silicon. So, intrinsic silicon will have some carrier concentration. This is the n i and n a is the carrier concentration of the substrate as I have already told.

So, based on that you can find out the threshold voltage by substituting different parameter values for a particular fabrication technology. Obviously, So, far as this part is concerned Q epsilon s I, K these are constants. On the other hand the C o x is the unit gate capacitance or these carrier concentrations you can will vary from process one process technology to the other process technology and as a consequence this threshold voltage will be different.

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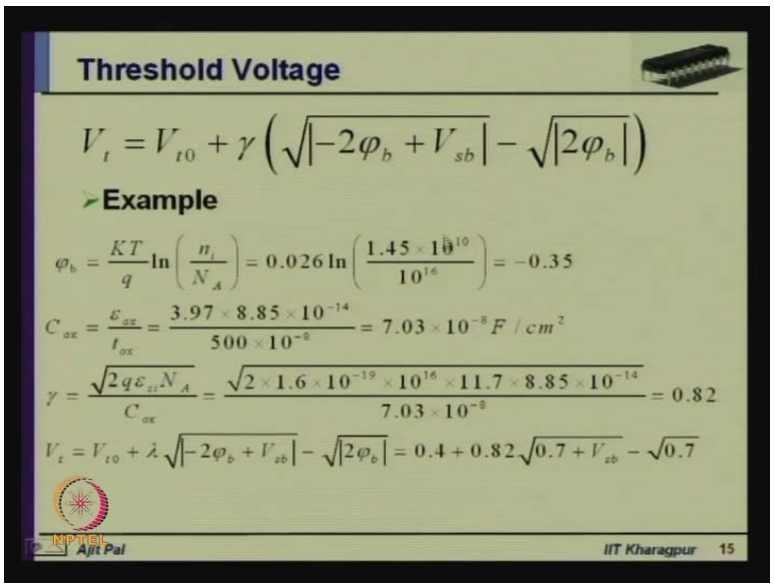

Now, let us take up an example. Let us see the, we can calculate the threshold voltage and we can see how exactly the threshold voltage varies as you vary the substrate bias phi b is equal to you can substitute different parameter values. This n i is equal to 1.45 into ten to the power ten centimeter. I mean per centimeter cube and n a is equal to 10 the power 16. So, 0.26 actually this K t by Q as you know is 26 millivolt. That is the K t

by Q value and this is the ratio of the n i by n a. Obviously, the intrinsic silicon has much layer lower carrier concentration compared to the carrier concentration of this substrate.

That means as you know substrate is uniformly doped to have more carrier concentration compared to the intrinsic substrate and phi b value is calculated. See this is the value of C o x. This phi b is minus 0.35 and C o x is equal to epsilon o x by t o x and this is the value 7.03 into 10 to the power minus 8 farad per centimeter square and you can substitute the various values to get gamma. Gamma is equal to, becomes 0.82. Here the value of the charge of electron the permittivity of silicon dioxide n a, these are all substituted and C o x these are all substituted and by substituting various values we get V t is equal to roughly 0.4. Assuming that 0.4 is the threshold voltage whenever the body bias is 0; that means, source is connected to the body and this part is is will this is the 0.82 this is your gamma into root 0.7 plus V s b. We have to take the absolute value and minus root 0.7. Now, you can actually vary V s b to get different different value of threshold voltage.

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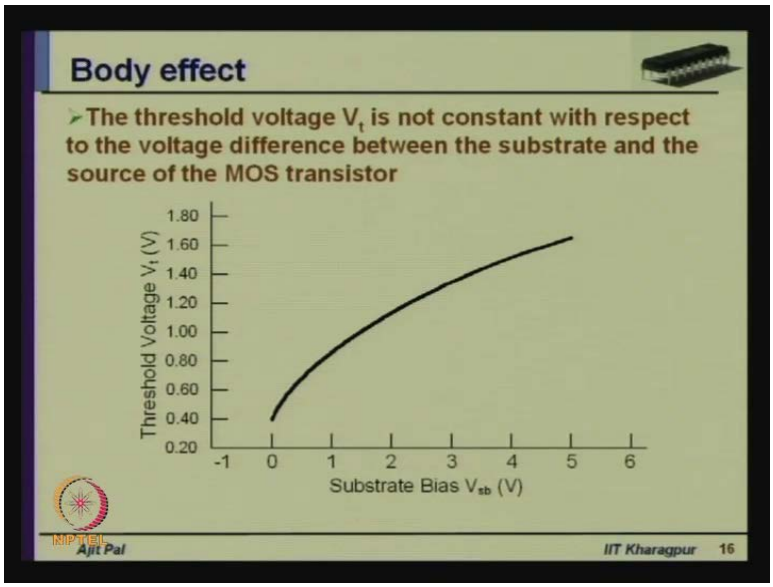

So, threshold voltage v t is not constant with respect to the voltage difference between the substrate and the source of the transistor. As you can see using that expression how the threshold voltage can change as you as you change the substrate body bias. So, you can see here, when the substrate bias is 0, as you have seen the threshold voltage is 0.4 volt. But, as you increase the substrate bias say from say 0 to 1 volt to 2 volt to 3 volt, it

can it can reach say 1.6. So, over a large range 0.4 to 1.6, a large change in the threshold voltage that can take place as you vary the threshold, the substrate bias with and threshold voltage will change and later on we shall use this and see how the threshold voltage can be controlled to reduce what is known as leakage current.

Because the leakage current is heavily dependent on the threshold voltage and later on we shall see instead of this positive bias, we shall usually apply negative body bias to low to to increase this. I mean with this is called the reverse body bias we shall do that to increase the threshold voltage such that the leakage current is lowered. That means, larger the threshold; voltage smaller is the leakage current. Smaller the threshold voltage larger is the leakage current. Later on we shall discuss more about it.

So, this is a body effect

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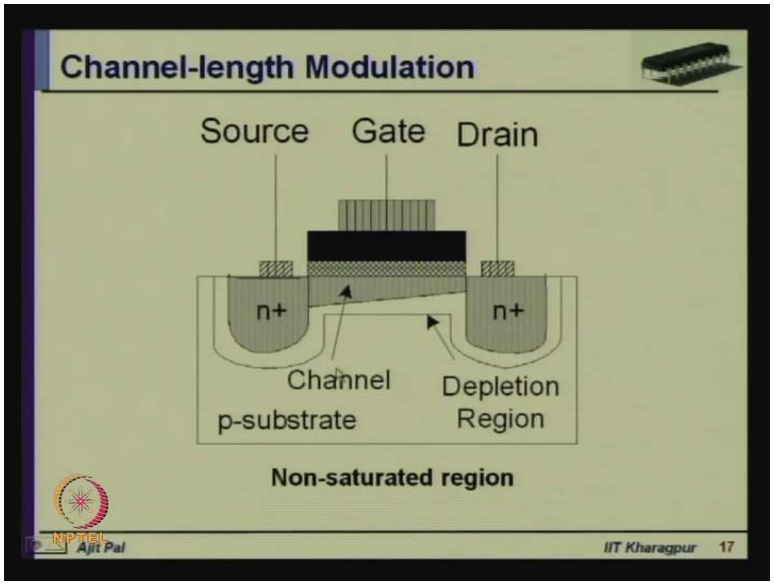

Now, we shall consider another very important parameter that is your channel-length rather phenomenon, channel-length modulation. Here in our expression for drain current, we have assumed that this l is constant fixed. It does not really change, but, in reality we will see this l is dependent on the drain voltage. However, this dependence is not visible until the channel-length is small. That means, it is, it becomes predominant in short channel devices.

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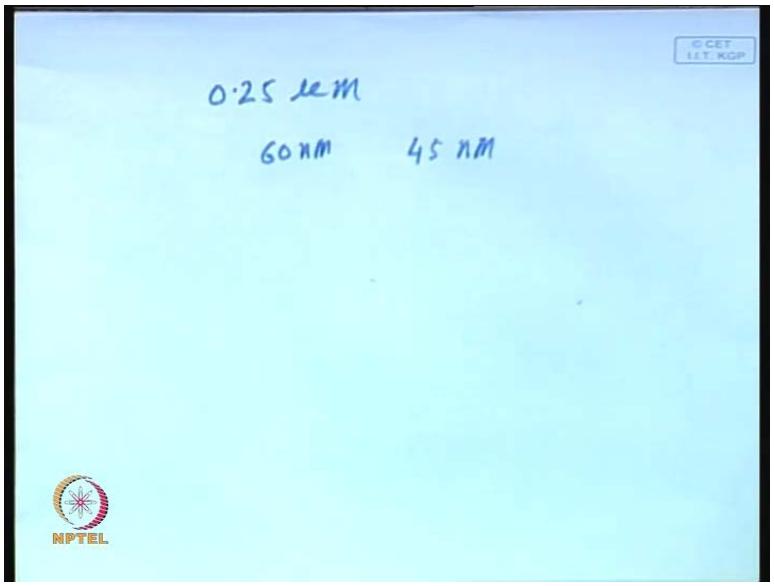

When the channel-length is say 0.25 micron 0.25 micron micro millimeter then this variation is so small that we do not really bother about it. But, whenever you are considering say sixty nanometer nanometer or say 45 nanometer technology instead of 250 nanometer technology, then this channel-length variation becomes visible or it cannot be neglected any longer.

First we shall show you why this variation (( )) take place. You can see the channel region is not uniform throughout the channel the reason for that is here the drain voltage is 0 here the drain voltage is high and because of the interaction between the gate voltage and drain voltage; the dense the the thickness of the channel region is not near the source and it is very narrow near the drain. And as we further increase the drain voltage what happens at some point of time the very close to the drain there is no carrier. That means, it becomes pinch-off. If we increase the drain voltage further, we will find that that that pinch-off point moves towards source. So, here there is small region where there is no charge carrier. So, essentially channel-length is now becoming smaller than the the physical length of the device.

So, effective channel-length is smaller and this is the, that is why we call it channel-length modulation. Essentially it is dependent on the drain voltage.

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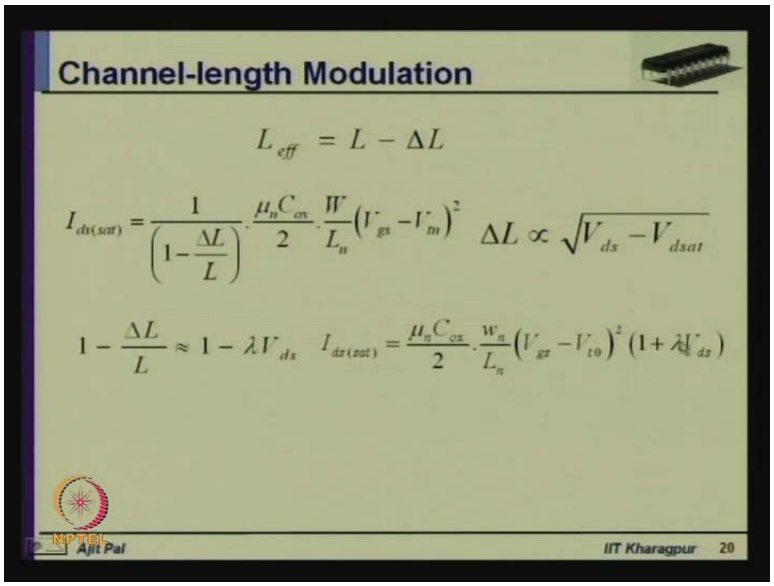

How do you take into account? We can take into account by substituting L effective which is equal to L minus delta L. So, n minus delta L is actually we can represent it by this we can represent it by this 1 minus this is the expression where we have substituted effective channel-length and we have got this expression. And this this variation is proportional to V d s minus V d sat. Essentially, when the saturation starts that is your V g s minus V t and this is the V d s. So, this change in the channel-length is proportional to the drain voltage. When the drain voltage is large only then this reduction occurs and this can be represented, this change 1 minus delta L by L can be represented by one minus lambda V d s where lambda is the is known as channel-length modulation coefficient.

So, we can now express I d s in term in terms of this lambda and it becomes like this, mu n C o x by 2 W n by L n into V g s minus V t square into 1 plus lambda V d s. So, you can see here, it is no longer one. It is here normally it is V d s. So, what it is 1 plus lambda V d s. So, it varies with drain voltage.

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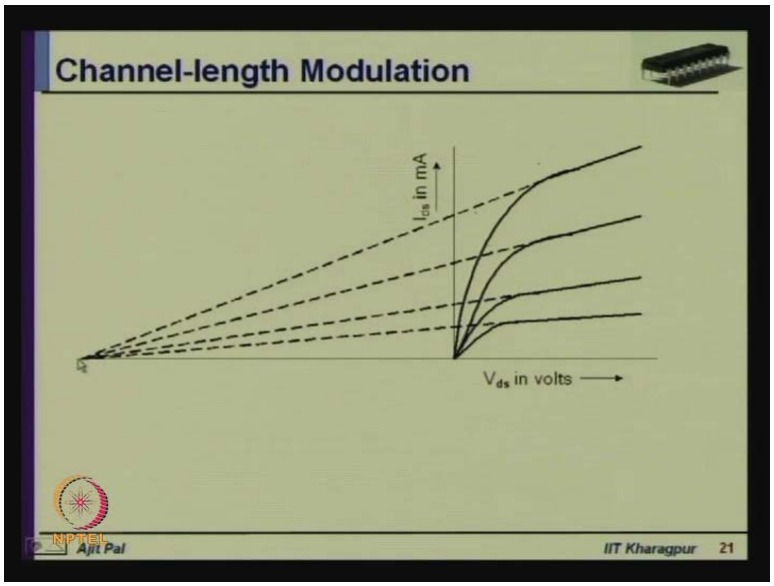

And this can be depicted pictorially with the help of this diagram as you can see in the saturation region, the although I have drawn it in a little exaggerated form, it will not be the slope will not be so high. What you can see the drain current is varying even in the saturation region because of channel-length modulation effect and you can see here it is becoming the it is no longer parallel, but, it is there is a point where it is touching and this is how the characteristic can be represented.

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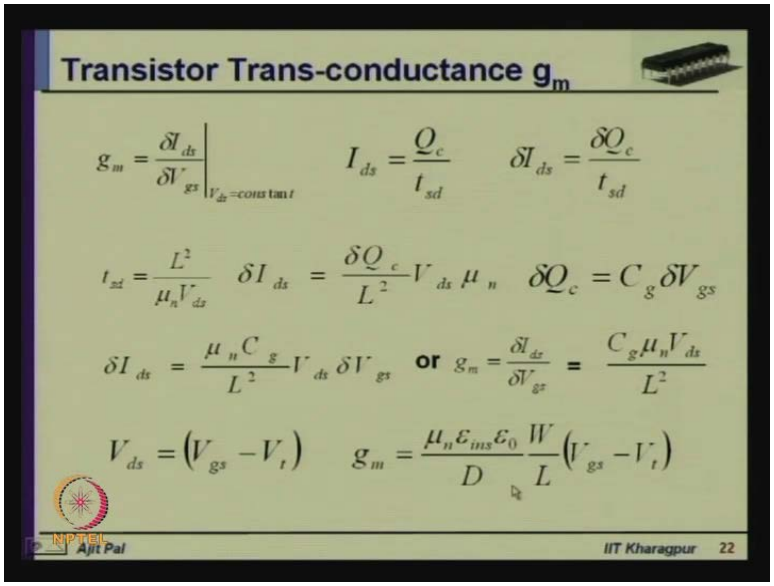

Now, another very important parameter that is known as transistor trans-conductance for bipolar junction transistors which is a current controlled device it is represented by gain of the transistor beta the collector current by base current. On the other hand in case of MOS transistors it is a voltage controlled device and similar parameter is known as trans-conductance. That means, rate of change of drain current by rate of change of gate voltage. So, here you have seen the the drain current is controlled by the gate voltage.

So, this trans-conductance is represented by delta I d s change of change of drain current by change of gate voltage delta V d s keeping the drain-to-source voltage constant. So, that we can derive as we know I d s is equal to Q c by t s D. So, delta I d s is equal to delta Q c by t s D and this is the t s D. That expression we have already derived I am not going into the details of that. So, delta I d delta I d s is equal to mu n C g s by L square into V d s into delta V g s and g m is equal to delta I d s by delta V g s, as we have seen which is equal to C g into mu n into V d s by L square.

And finally, by substituting V d s is equal to V g s minus V t, we get g m is equal to mu n epsilon I n s into epsilon 0 W by D into L into V g s minus V t. So, you can see the the gain which is represented by transistor trans-conductance. More the gain it is better. We can see it is dependent on the mobility of the device, width of the device, thickness of the silicon dioxide length of the channel and the effective gate voltage which is equal to V g s minus V t. So, this is the parameter and we can, how we can increase the value of g m is clear from this expression which parameter we can really; that means, if the width is more more current will flow. So, that is why g m will be more. If the thickness is small of the silicon dioxide gate voltage you will have more control and obviously, g m will be large. Similarly, the length is small more current will flow. So, g m will be increase. So,

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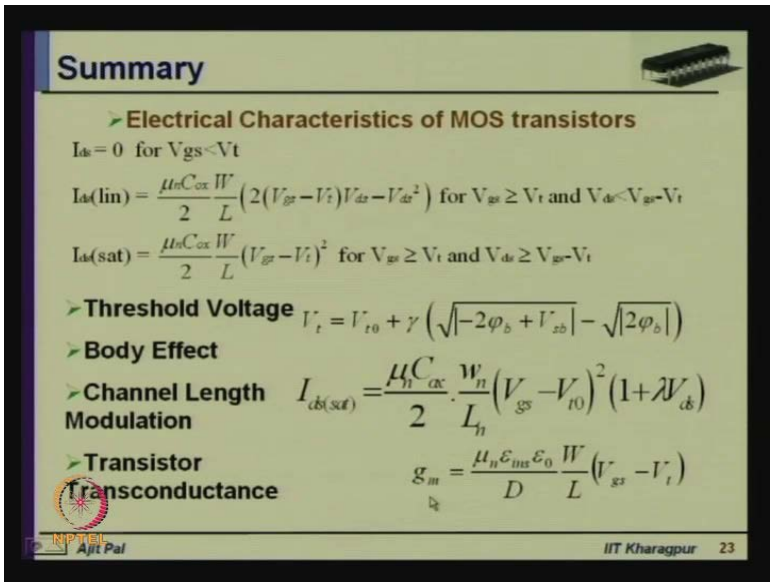

So, here we can summarize. We have discussed about three regions of the operation of MOS transistor. We have derived the expression of threshold voltage and explained what is known as body effect and we have also considered channel-length modulation phenomenon and then explain what is known as transistor trans-conductance. So, with this, let us stop here. In the next lecture we shall discuss how a transistor can be used as a switch. Thank you.