Low Power VLSI Circuits and Systems

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Lecture No. # 02

MOS Transistors - I

Hello and welcome to today's lecture on MOS transistors, this is the first lectures on this topic, as I mentioned in the last lecture our course will be based on CMOS circuits, because CMOS is the technology of choice today. And we shall follow it bottom of approach, in the bottom of approach as you know, we start with very simple things and we shall start with MOS transistors, and then we shall gradually discuss MOS invertors MOS complicated circuits and other things.

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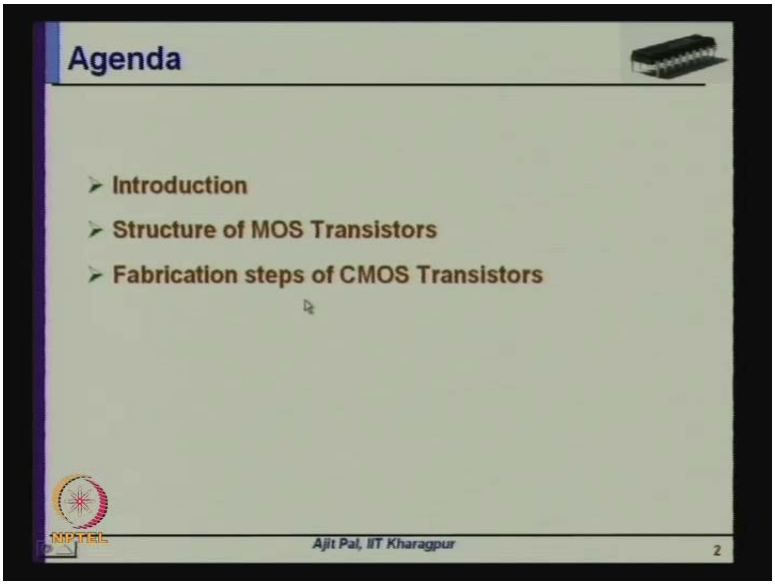

And so today is a first lecture on MOS transistors, and here is the agenda of today's lecture after giving a brief introduction, I shall discuss structure of MOS transistors. You will see there are different types of MOS transistors available, and I shall discuss all of them one after the other. And then I shall discuss fabrication steps of CMOS transistors, because this understanding of this fabrication step is necessary to know about how

actually CMOS circuits are realized, and then what are the complicacy, I mean complications and steps involved in it.

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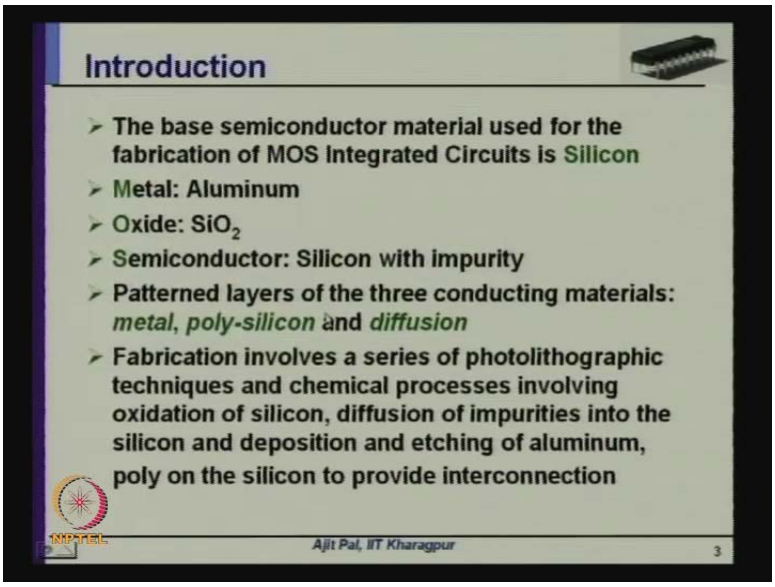

As you know the best semiconductor material used for the fabrication of MOS integrated circuit is silicon. Silicon is the material is a material which is available in abundance in nature and it is very cheap. So, there is no dearth of raw material in the nature you get plentiful of I mean silicon in the form of silicon dioxide or sand. However, you have to use a very purified form of silicon for the fabrication of VLSI circuits. So, usually by reacting silicon dioxide or sand with carbon, the silicon is purified to a great extent then it is used for the purpose of fabrication of VLSI circuits.

And here we shall be using the term MOS. What do you really mean by MOS? A MOS stands for metal oxide semiconductor you will see, these transistors are realized by using three different types of material one is metal, metal is usually aluminum or some time polysilicon is also used for the purpose of conductions, conducting material and oxide is your silicon dioxide which is used as an insulating layer and semiconductor is silicon with impurity as you know silicon in the pure form is not a conductor is an insulator however, you have to add some impurity to realize I mean to make it semiconductor that means, it will be partially conducting and then it will be creating pattern layers of three conducting materials.

The conducting materials are metal in the form of aluminum and then polysilicon which is also a conducting material, which is used for making interconnections among different parts of the circuit then diffusion, diffusion is also a conducting layer which will be created by two usually two processes another one process is known as diffusion another is aluminum plantation then these three layers are actually, I mean realized one after the other using silicon dioxide as an as an interfeeding layer in the in the form of a sandwich. So, the sandwich like structure of is realized to implement MOS transistors and we shall see the fabrication of MOS transistors involved a series of photolithographic techniques and chemical processes involving oxidation of silicon to implement to realize silicon dioxide diffusion of the impurities into the silicon to implement n plus or p plus regions and deposition and etching of aluminum that means, which used for the purpose of interconnecting different layers, so etching of aluminum polysilicon on poly on the silicon to provider interconnection.

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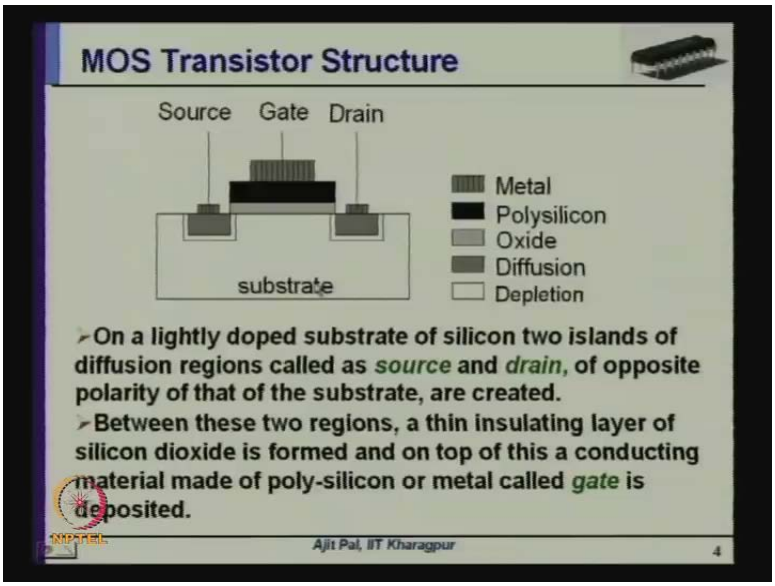

So, with this brief introduction let us have a look at the structure of a MOS transistor. So, as you can see this simplified diagram of a MOS structure which is shown here it has got two regions this is the substrate, the substrate is either lightly doped p type or n type here I have not shown any anything, but it can be either p lightly doped p type or lightly doped n type and then I have got it will be creating, I mean two highly doped regions islands you can say which are known as source and drain.

So, on a lightly doped substrate of silicon two islands of diffusion regions called source and drain and this source and drain which are heavily doped are of opposite polarity of that of the substrate, so that means, if the substrate is lightly doped p type then these diffusion regions that means, source and drain will be of n type n plus type and these are known as source and drain as you can see here and of course, for taking interconnection you can see metal layer has been deposited for interconnecting two other parts of the circuit then between these two islands source and drain a thin insulating layer of silicon dioxide is formed, you can see this is a thin layer of silicon dioxide which is also known as thin ox thin layer of silicon dioxide and on top of this a conducting material made of polysilicon, this is a polysilicon layer which has been deposited on this thin layer of silicon dioxide and then on top of the polysilicon you can deposit metal for making interconnections and this forms the gate that means, on top of the polysilicon the metal layer is deposited and this forms the gate, now this is the structure generalized structure of a MOS transistors and as I told you have two alternatives you can have either a p type substrate or n type substrate.

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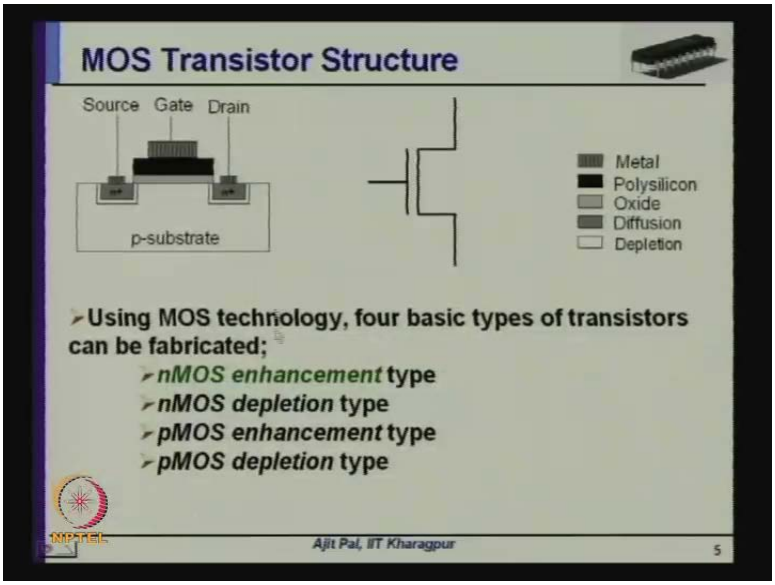

So, whenever you are using p type substrate and these heavily doped regions are n type called n plus and n plus, then we realize nMOS transistor. Now, the MOS transistor operation is based on the flow of current in this channel region, which is under this silicon dioxide layer this is the channel region this flow of current between source and drain in this channel region, now you see in this form; in this original form there cannot

be any flow of current because flow of current requires some carrier, so in absence of any carrier there cannot be any flow of current. So, you have to create some carrier charge carrier, so that current can flow in this channel region and for that purpose there are two different techniques are used on is known as enhancement mode in this mode what is being done a positive voltage is applied on the gate and whenever a positive voltage is on the gate, it will induce charge of opposite polarity on the other side of the silicon dioxide, so in this region in this channel region charge of opposite polarity will be induced or in another words an inversion layer is created, so that inversion layer is made of electrons in this particular case and then electrons forms the channel.

I mean the channel in this region that electrons is can be used to carry current between source and drain since, in this particular case you are applying a voltage to create the channel that means, you are creating an inversion layer and by controlling the gate voltage the flow of current between the source and drainage carried out and that is the region why it is called n MOS enhancement type transistor. So, in this particular case originally there is no charge carrier, but you are applying a positive voltage of sufficiently, I mean sufficiently high positive voltage to create charge of opposite polarity in this particular case of electron for the flow of current between source and drain, now is it the only way of creating the conducting path another alternative.

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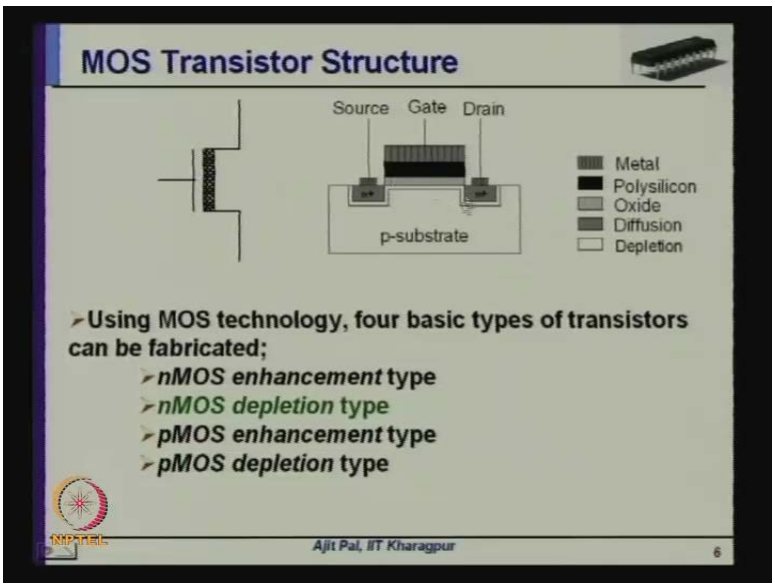

There in which case by you can create the channel region you can actually you can implement by using an implantation you can create electrons you can put electrons in this region that means, in the absence of any gate voltage a channel is formed and electrons are available in this region and as a consequence even when the gate voltage is zero, current can flow between source and drain and you may say that in this particular case how do you really stop the flow of current? What you can do, you can apply a negative voltage to the gate and; obviously, if you keep on increasing the negative voltage on the gate then it will gradually deplete this region; that means, depletes the region from the charge carriers; that means, the electrons which have been deposited here will be removed, whenever a negative voltage is applied and that will induce holes and holes will actually remove these electrons. So, here also that means, by applying a negative voltage starting from zero to some negative voltage, you can control the flow of current between the source and drain, so thus you have realized a nMOS depletion type transistor. So, basic structure remaining same except you is here at the time of fabrication you are creating the channel region by diffusion process.

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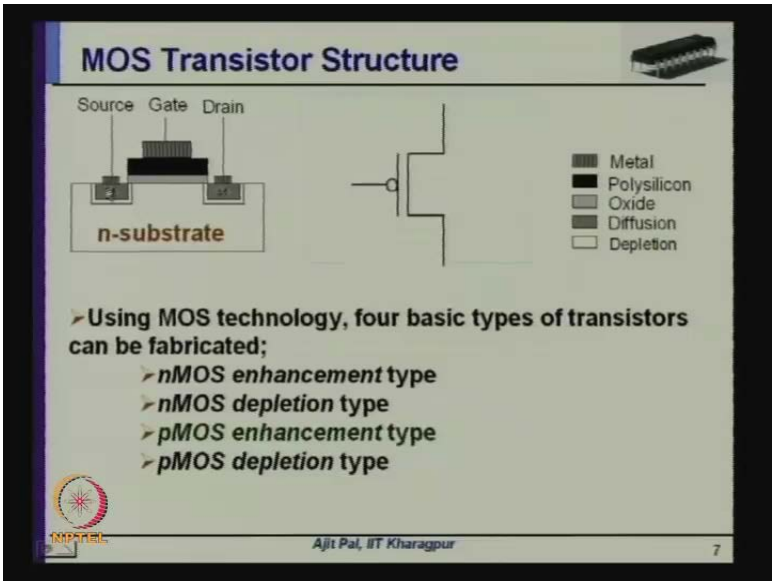

Then let us come to the third alternative, where you are starting with a n type substrate that means, this is a lightly doped substrate and then in this case these heavily doped regions will be off p type that means, here it will be p plus and p plus which will form the source and drain here also you have got two types pMOS enhancement type. So, in this in this case there is no I mean flow of current when the gate voltage is zero, but if

you apply a negative gate voltage respect to the source and if the gate voltage is sufficiently high, it will induce holes in this region and that will and the hole will holes will act as charge carrier, I mean current carrier between the source and drain and current can flow between the source and drain and this is how the pMOS enhancement type transistor is realized and I have not shown the symbols here you can see there is a symbol of a nMOS enhancement type transistors there are different several types I mean, different types of symbols used in the literature, but this is the most commonly used symbol of nMOS enhancement type transistor similarly this is the most commonly used symbol of nMOS depletion type transistor and then this is the most commonly used symbol of pMOS enhancement type transistor, then the fourth type of nMOS transistor that is you pMOS depletion type in this case just like the nMOS depletion type the holes are implanted in this region to create to have channel even when the gate voltage is zero and then you can apply a positive voltage to the gate to gradually reduce the number of charge carriers in this channel region and you can in this way you can control the flow of current.

So, you can have p MOS depletion type transistor, so you can see you can have four different types of transistor nMOS using MOS technology, nMOS enhancement type, nMOS depletion type, pMOS enhancement type and pMOS depletion type, now one at this point I should tell you about another important point, you can see in this particular case the current flow take place by controlling only one form of charge carrier; that means, either you are controlling the electrons, electron is taking part in the flow of current or holes are taking part in the flow of current; that means, in case of nMOS transistors the electrons are taking part in the flow of current, on the other hand in pMOS transistors the holes are taking part in the flow of current and that is the reason why most devices are known are unipolar devices.

In contrast to bipolar devices you know, those bipolar devices those are realized by using say junction transistors for example, those are bipolar devices, because the current flow take place by the by current flow can take place and where both electrons and holes take part; that means, current flow occurs because of electron hole recombination that does not occur in case of MOS devices and that is the reason why MOS devices are known as unipolar devices. So, let us switch gear and let us have discussion on fabrication steps of CMOS transistors, so we have seen different types of MOS transistor structures how do

you really fabricate them this is interesting and; obviously, we cannot really devote much time on it, but remaining part on this lecture I shall devote to fabrication steps of CMOS transistors.

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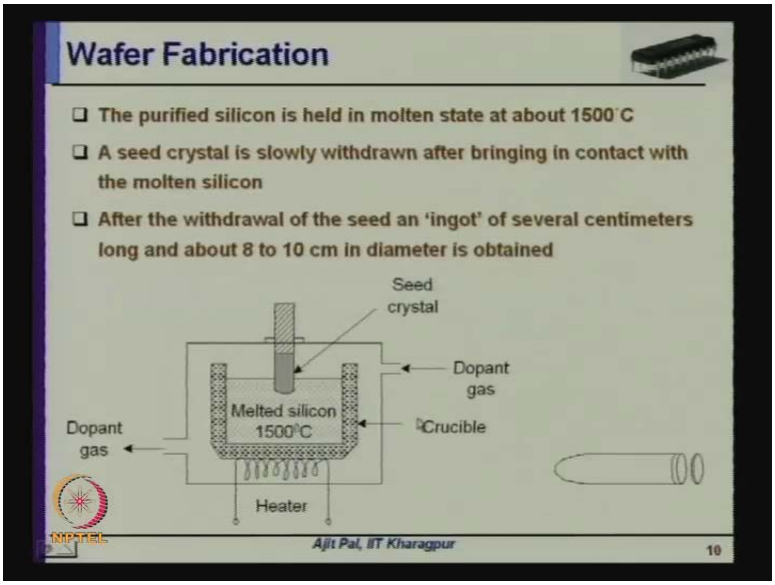

So, as I have mentioned the first step is the realization or creation of a wafer, so wafer is the material which is also called a substrate on which the VLSI circuits are fabricated how's it realized? So, what is being done the purified silicon is held in molten state at about 1500 degree centigrade as you can see in this cubicle, the crucible in this crucible the silicon is kept in molten form and it is it is in very highly purified form, how the purification is done? That I have not discussed, but I have already mentioned that by reacting with carbon you can create the create highly purified form of silicon. So, which is kept in a molten form, so this is the silicon at 1500 degree centigrade and now what you do a seed crystal is slowly withdrawn after bringing contact with the molten silicon.

So, here is a seed crystal which is slightly dipped in this molten silicon, then it is gradually withdrawn very slowly as it is gradually withdrawn, the molten silicon comes in contact with that and it gets it gets attached to this seed and takes the takes the crystalline form and as a result as you gradually withdraw it from the molten silicon and ingot in this form is created in addition to this whenever, you do the withdrawal that time you usually insert some do pant gas inside this chamber what is a purpose of this do pant gas? As I mentioned whenever you do the fabrication the wafer has to be either slightly

doped lightly dope p type or n type how do you really get this lightly doped p type or lightly do pant type this is done at the step; that means, do pant of suitable type is bust through this chamber as you can see it is introduced here and is coming out from here.

So, it is introduced in this chamber and as a consequence the that you get is essentially lightly doped p type or n type it can be either way it can be done in any one of the two ways then after the withdrawal of the seed and ingot of several centimeters long 3 to 4 centimeters long and 8 to 10 centimeter in diameter is the obtained then these this ingot is sliced you can see this is sliced. So, this is this forms the wafer, so this slice after slicing this ingot we get a number of wafers and the wafer is the best material that is being used for the purpose of fabrication.

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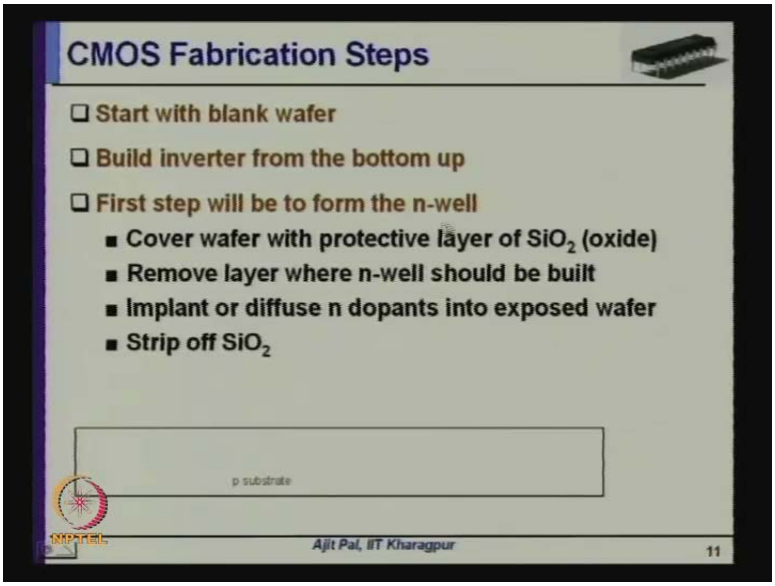

Then you have to follow a number of steps for the purpose of fabrication of MOS transistor, so you start with blank wafer build inverter from the bottom up. So, which I will show how the inverter can be realized, but you can create more complicated circuit, but here I shall show the formation for an inverter simple inverter, so first step will be to form a n-well, so you know the most common type is n-well, so you have started with a p type substrate and as you know on a p type substrate you can realize nMOS transistors depletion type or enhancement type, but CMOS will require both n MOS and CMOS as I have told you can have four different types of transistors.

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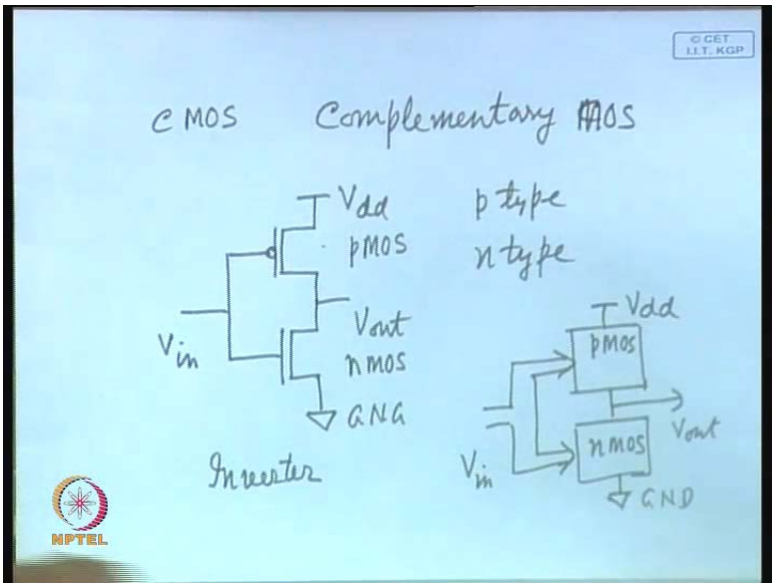

Then C MOS which stands for complementary MOS requires two types of transistors one p type transistor, another is n type transistor for example, a simple inverter will require a p type, here it is from the symbol it is very clear the it is a p type enhancement type transistor you will also require a n type nMOS transistor. So, these two together will from an inverter, so here you will apply v d d here you apply ground and then you will, you will apply the input here you will take the output from here.

So, you can see a complimentary MOS circuit requires two types of two complimentary types of transistor one is p MOS which acts as pull up network and the n MOS transistor will act as pull down network, so here it is a very simplified form of circuit that is your inverter you can create very complex circuit in that case the generalized structure will be like this you will have a pMOS network and will have another network nMOS network and you will apply inputs to both pMOS and nMOS network and you will take the output from here.

So, here is the various inputs and here is your output and of course, this pMOS network is connected to v d d ground and nMOS network is connected to ground and pMOS network is connected to supply voltage v d d, so this is the complimentary CMOS so we shall see the fabrication of this inverter how it is being done, so first thing to be done is to form an n-well why do you require an n-well, because you will require a pMOS

transistor as well for the realization of CMOS circuit and these are the steps cover wafer with protective layer of silicon dioxide then remove layer where n-well should be built.

So, this will require two steps cover wafer with protective layer of silicon dioxide how it can be done? That can be done by a process known as oxidation. Oxidation can be done by heating this wafer the substrate in a chamber like this one heating chamber like this one and then by passing either oxygen or water vapor, so whenever you are passing oxygen then it is called dry oxidation then thin form of silicon dioxide is created on the other hand whenever, you will be passing I mean seeing the water vapor then thick form of silicon dioxide will be deposited, but it is quality will not be very good it will be little porous type and it is called thick oxide silicon dioxide.

So, you can use either oxygen or water vapor for the purpose of in the oxidation process and to realize the silicon dioxide layer on top of this substrate, then remove the layer where n-well should be built this removal of n-well from the I mean removal of silicon dioxide, where n-well should be formed requires a photolithographic process and then you will implement a diffuse n do pants into exposed wafer and then you will strip off silicon dioxide.

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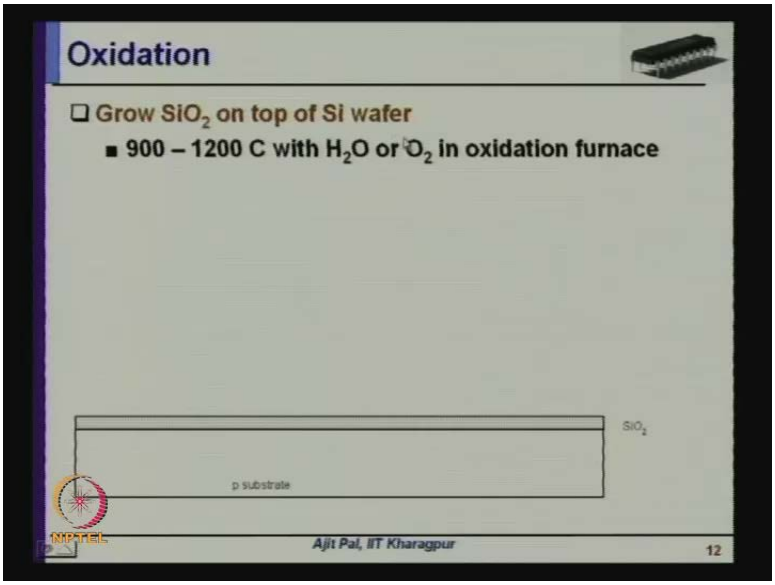

So, you can see you are starting with substrate then you are growing silicon dioxide on top of the silicon wafer how it is being done 900 to 1200 degree centigrade it is heated and with either water vapor or oxygen in the oxidation furnace as I have already told.

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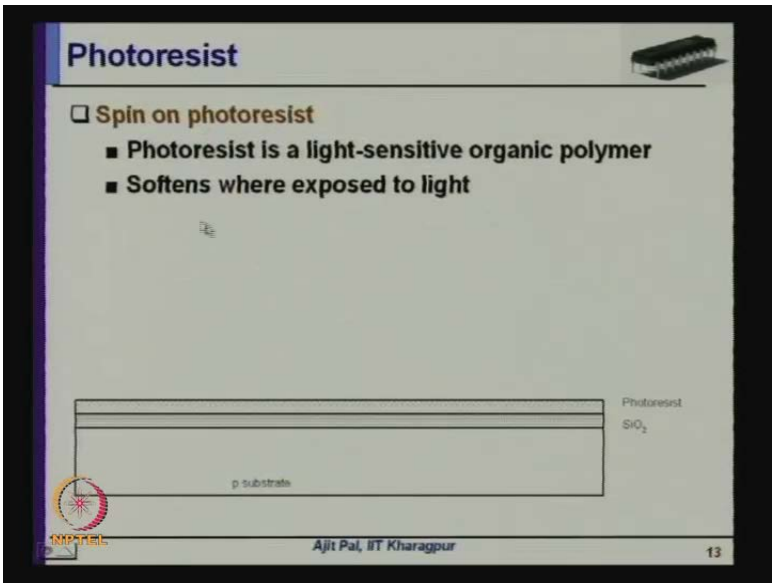

And after that you do the photolithographic process that means, you deposit I mean photographic emulsion photo resist on top of the silicon dioxide and then it is spread uniformly by spinning it at little high speed, then you expose it to light with the help of a mask.

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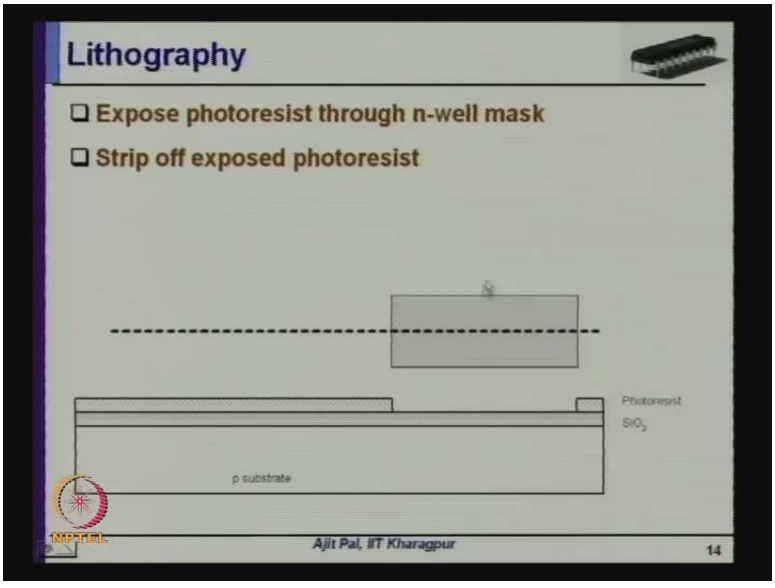

So, you require a mask and this portion is not exposed as you can see and then after this portion is not exposed, so this photo resist can be easily removed from here and after that

by a process known as etching the silicon dioxide will be removed etch oxide with hydrofluoric acid.

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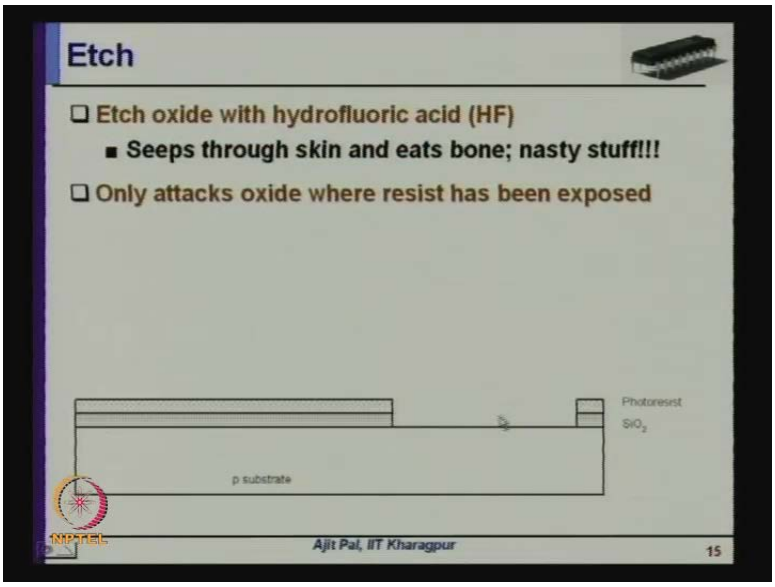

So, by reacting with this hydrofluoric acid this silicon dioxide is removed, so you have now exposed substrate here and actually this etching process you are using a chemical such that it reacts only with the silicon dioxide; not with the silicon, so only attacks outside when resist has been exposed, so this portion is silicon dioxide is removed, but not the top portion.

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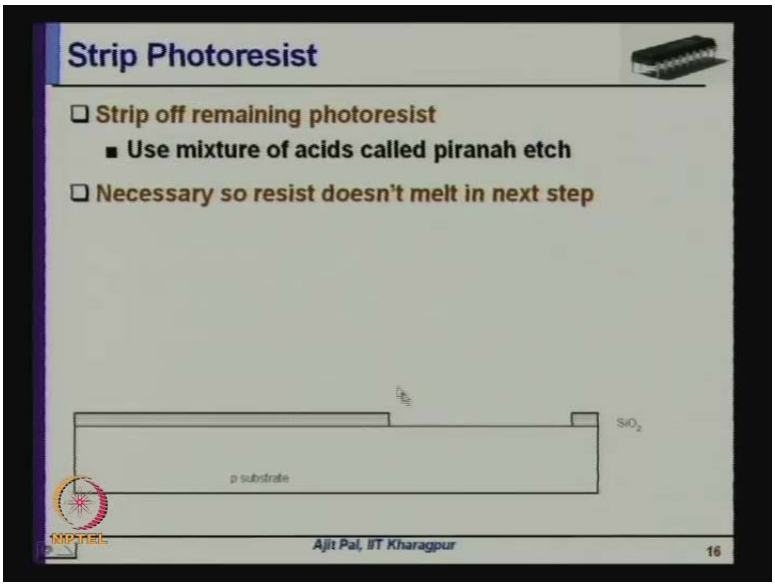

Then of course, you will remove the strip off the remaining photo resist use mixture of acids called piranha etch, so this is this is another etching process where you have removed this photo resist from the from the top of the silicon dioxide layer then necessary to resist. So, it is necessary to show resist does not melt in the next step then

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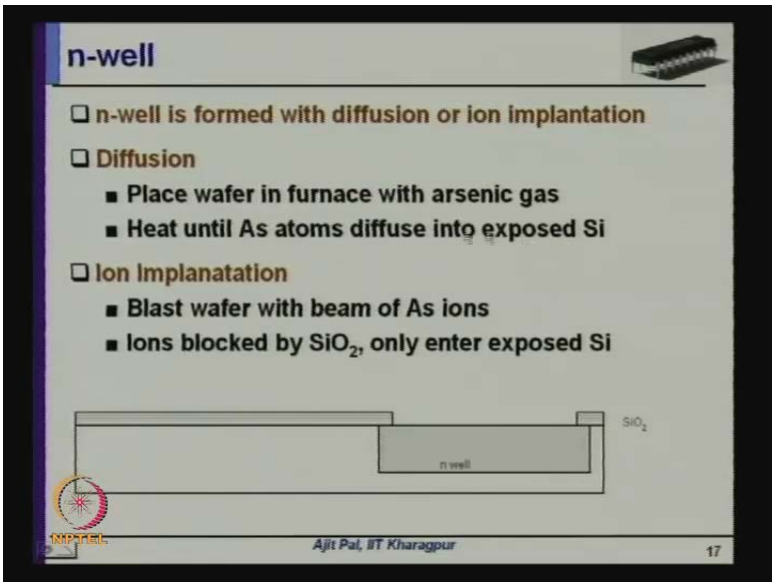

What you will you do? You will form the n-well is formed with diffusion or ion implantation as I told there are two types or two ways of realizing diffusion region one is you can again put that wafer in a chamber and you can pass suitable do pant through that chamber and it is heated at a very high temperature and after some time you have to give suitable time, I mean time of suitable duration such that the do pants can penetrate after certain layer and after that you have to do, what is known as drive-in process you have to simply heat it up for certain duration, so that the do pants can get stabilized and gets uniformly distributed within that certain region.

So, these are the two steps place wafer in furnace with arsenic gas this is the do pant used for the for this purpose for the creation of n-well and heat until arsenic atoms diffuse into exposed silicon this is the drive-in process, another alternative as I told is ion implantation either of the two can be used blast wafer with beam of arsenic ions blocked by silicon dioxide only enter exposed area that means, here you know this silicon dioxide is now acting as a kind of protecting layer. So, only this part will be will have the diffusion and this the other part will not have the diffusion that means, the arsenic ions

will be will be able to pass through this exposed area, but not through the silicon dioxide layer, so this is how the n-well is formed so you have got lightly doped area of p type and lightly doped area of n type.

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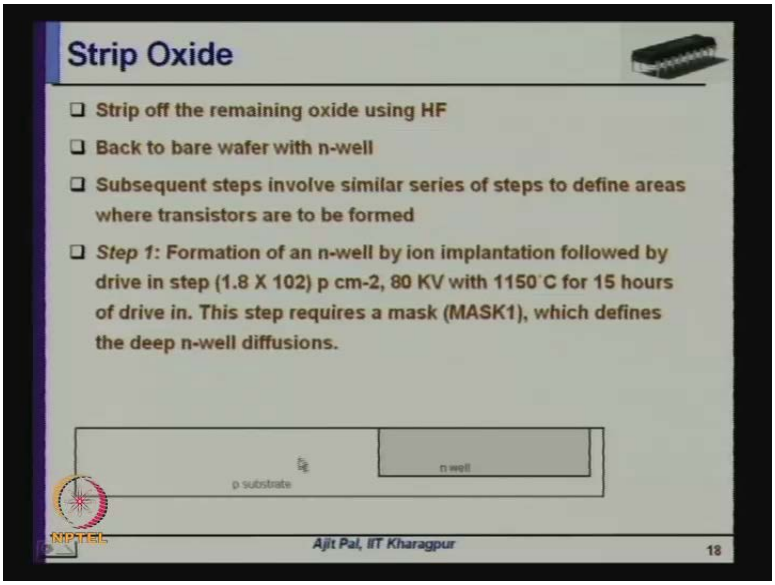

So, where you can create two different types of transistors, so now you have the substrate with n-well, so strip off the remaining oxide using hydrofluoric acid, then back to bare wafer with n-well, so this is what is being shown in this diagram. So, subsequent steps involve similar series of steps to define areas where transistors are to be formed, so formation of n-well by an ion implantation followed by drive in step as I have already told this step I have already discussed this is done by using MASK one.

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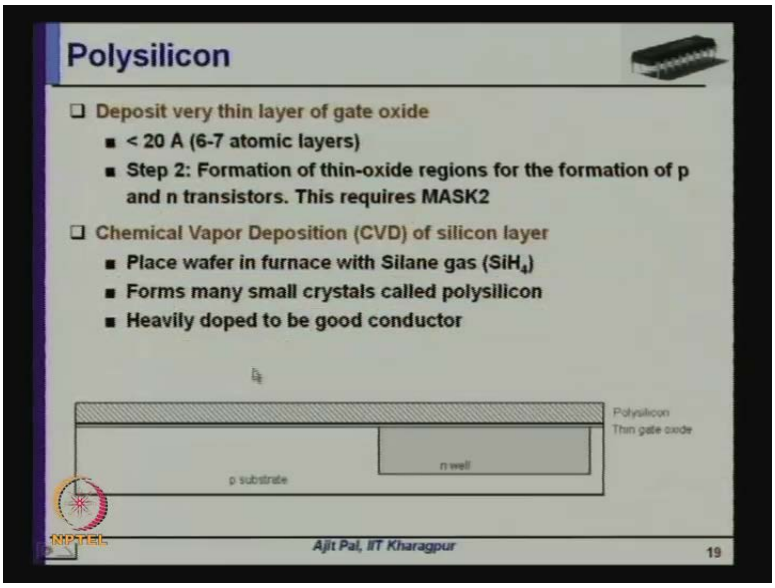

So, this is the MASK 1, this is the MASK 1 and coming to the second step which requires formation of polysilicon layer so deposit very thin layer of gate oxide, so first step is very thin layer of silicon dioxide is deposited again by that dry oxidation process as I told it will be heated in a furnace and oxygen will pass through this chamber and thin silicon dioxide layer will be formed. So, this is what is being done to clear the thin oxide layer and then on top of that we will deposit polysilicon layer and polysilicon layer is deposited by using a technique known as chemical vapor deposition or CVD on the, on the on top of this silicon dioxide layer.

So, for this purpose what you have to do you have to place wafer in a furnace with silane gas from many small crystals like polycrystal, polysilicon, polycrystalline layers and heavily doped to be good conductor since this is heavily doped. So, it will form a good conductor because this will be used for the purpose of interconnection, so this polysilicon must be a good conductor relatively good conductor because it will be used as a interconnection layer to connect different parts of the circuit.

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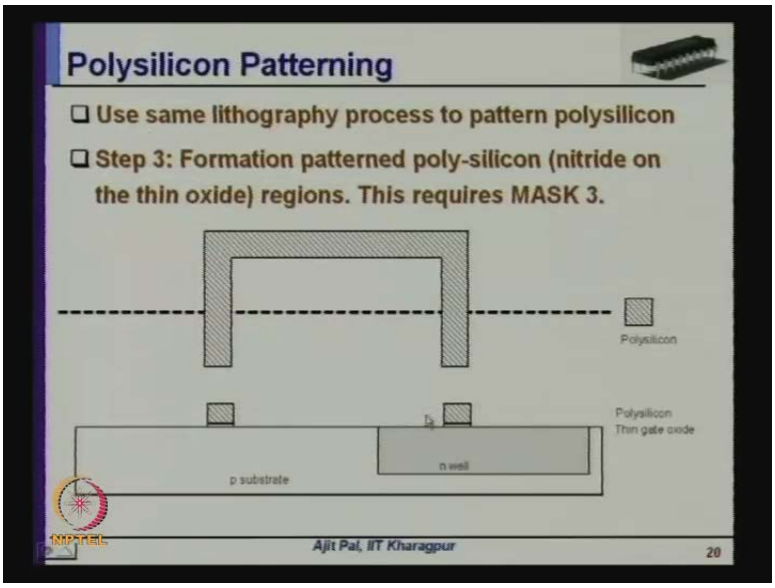

So, this is what this is another MASK is used for the purpose of creating that pattern polysilicon layer, so use the same photolithographic process to pattern polysilicon, so earlier for the polysilicon was deposited on the entire surface, now you have to create a patterned layer with the help of this MASK called MASK three. So, formation of patterned polysilicon regions and you can see only polysilicon is present in these layers and from other parts of the substrate polysilicon has been that means, only where transistors are to be formed there the polysilicon is deposited.

So, it is removed from the remaining portion, so you can see here essentially that gate has been formed gate portion, so this is the gate of the n MOS transistor this is the gate of the pMOS transistor, so here you got thin oxide layer and the polysilicon layer, here also thin oxide layer and polysilicon layer only difference is here you have got the lightly doped p type substrate and here you have got lightly doped n type region within the n-well.

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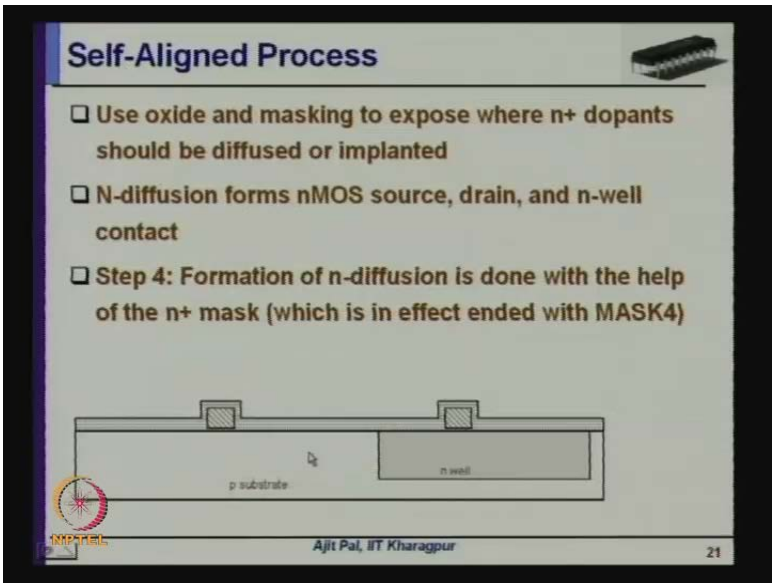

Now, what you have to do you have to clear diffusion you have to clear those you know source and drain regions. So, you have to use oxide and masking to expose where n plus do pant should be diffused or implanted. So, either you will use diffusion process or ion implantation to realize those source and drain regions, so n diffusion n MOS source drain and n-well contact and formation of n diffusion is done with the help of an n plus mask which is in effect ended with MASK four, so you have got another mask or mask four to realize to define those you know that those source and drain of the n MOS transistors.

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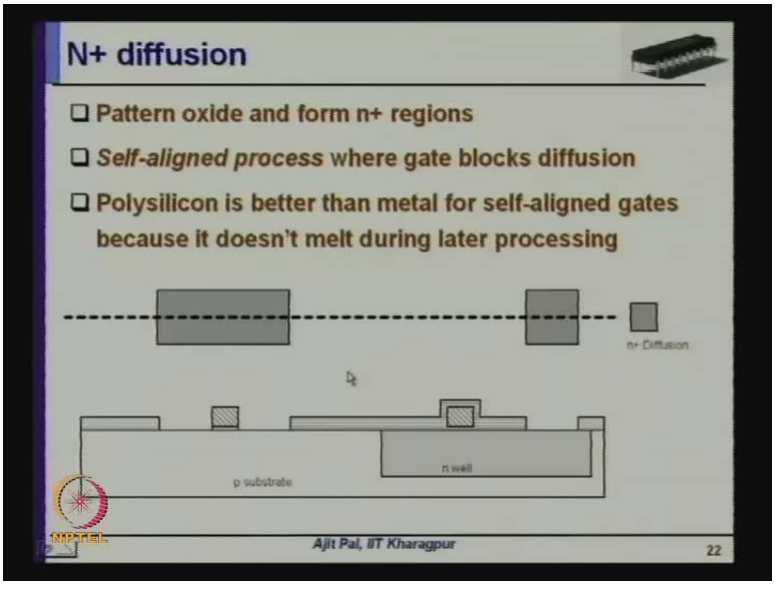

So, pattern oxide with form n plus region, so this is the mask of the n diffusion and this is self-benign process where gate blocks the diffusion, so here you can see this portion there will be no diffusion and the polysilicon and the thin silicon dioxide will protect the this the channel lesion, where channel lesion will form and only these two areas will be will have the source and drain regions heavily doped regions when you carry out those diffusion or ion implantation.

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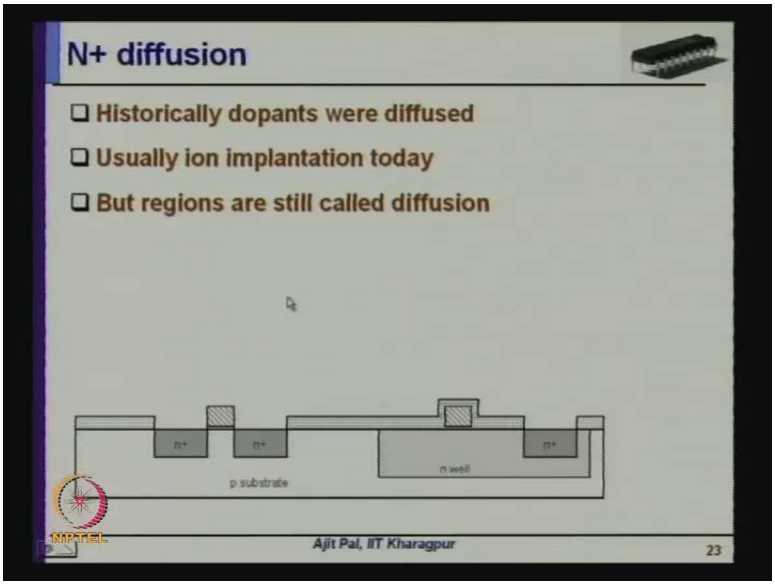

So, now you have done that n plus diffusion, so as I told historically do pants were diffused by the diffusion process, but nowadays ion implantation is the technique which is commonly used because of its high accuracy, you know diffusion whenever you do the diffusion then the these regions are not very accurately defined on the other hand, by using because these days these lines will not be straight lines. So, it will be somewhat like this, somewhat like this, but whenever you do by using ion implantation then you can create those n plus regions very nicely, so you can see three n plus regions have been created source and drain another is n-well contact here n plus region you have to actually connect this n-well to v d t and for that purpose n plus region is created here, so these three are created by this n plus diffusion.

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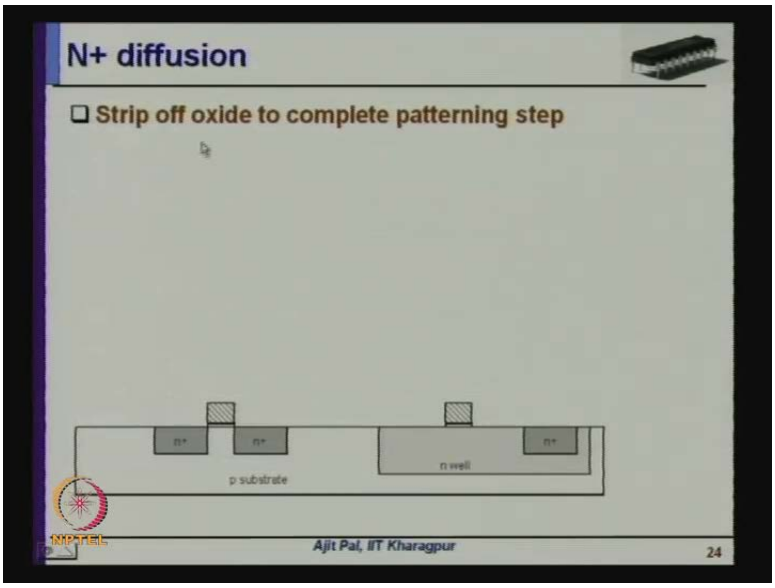

Then you have to strip off oxide to complete patterning process, oxide is removed which was acting as a protecting layer for the other parts of the substrate.

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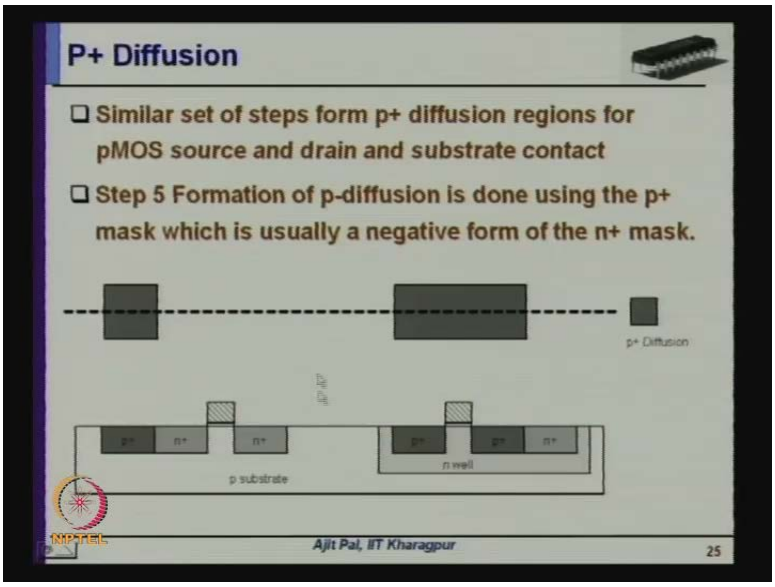

Then you have to do p plus diffusion, so for the purpose of p plus diffusion you will require another MASK, so this is your step 5, so you have to follow the similar steps to form p plus diffusion region, only difference is you have to use a different kind of do pant, do pant type will be different and formation off n diffusion is done using p plus mask which is used with a negative form of n plus mask because as you know where you

will create nMOS transistor there you will not create p plus transistor. So, just the opposite that is the reason why these two are of opposite type and negative of n plus MASK, so essentially to save the cost of making the MASK.

So, this is this is how the p plus diffusion is done as you can see here p plus diffusion is done in three regions first the that source and drain region of the pMOS transistor and also another p plus region is created here to make contact with the p substrate because you will see later on that the substrate has to be connected to ground, then the substrate has to be connected to ground and to make contact with that substrate this p plus region is created, so you can see three p plus regions have now created and, so you have got a nMOS transistor a pMOS transistors in addition to two contacts one for connecting the substrate to ground another for connecting the n-well to power supply or v d d now you will you have to make a circuit, so far here you have got two transistors you have to interconnect them to form an inverter, or some you have to in the inverter may be part of a more complicated circuit.

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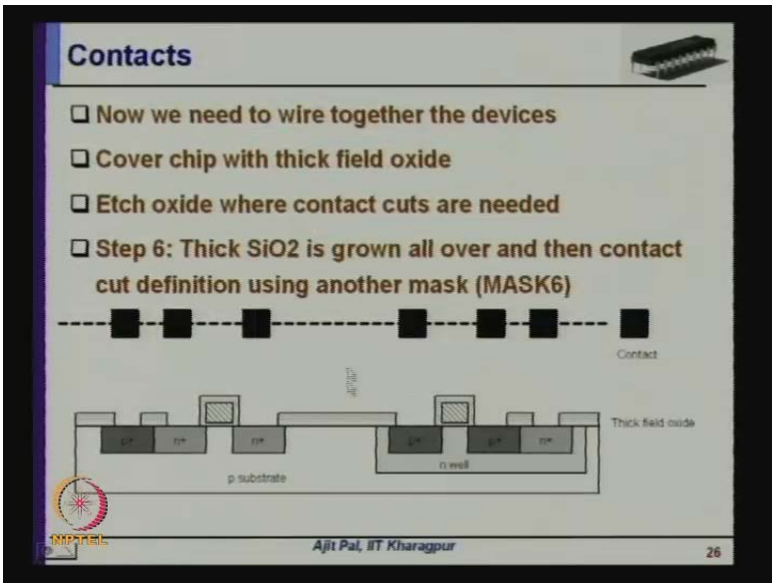

So, you can see here you have to now make contacts, so another MASK is required, so thick silicon dioxide is grown all over and then contact cut definition using another MASK 6. So, you will require a separate mask to create contacts, I mean wherever you have to make contact with other parts of the circuit mask is created accordingly, so now you need to wear together the device; that means, all the devices are to be wed together

using this and for that purpose you will require these contacts cover chip with thick field oxide. So, this thick field oxide is created by usually by wet oxidation as I have discussed earlier then h oxide where contacts current cuts are needed again by using that photolithographic process you will make those you will remove those thick oxide layers from these regions where contacts has to be established.

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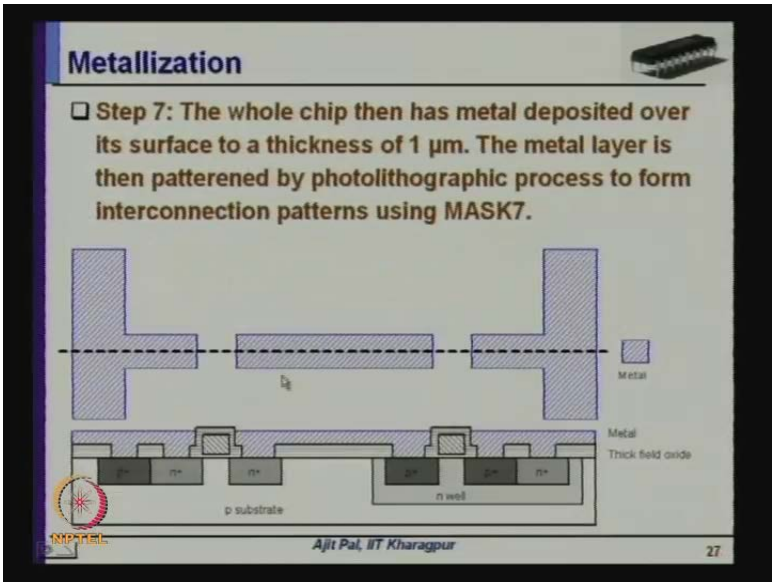

And then for making the contact you have to do I mean you have to use a metal layer, so for that purpose entire chip entire substrate will be covered with metal usually aluminum, so the whole chip then has metal deposited over its surface with thickness of one micron, the metal layer is then patterned by photolithographic process to form interconnection pattern using MASK 7. So, you will require another MASK to define the interconnection pattern, so you may have to connect that inverter to another part of the circuit, so input has to come from one part, output has to go to another part of the circuit, so that is being defined with the help of this MASK 7.

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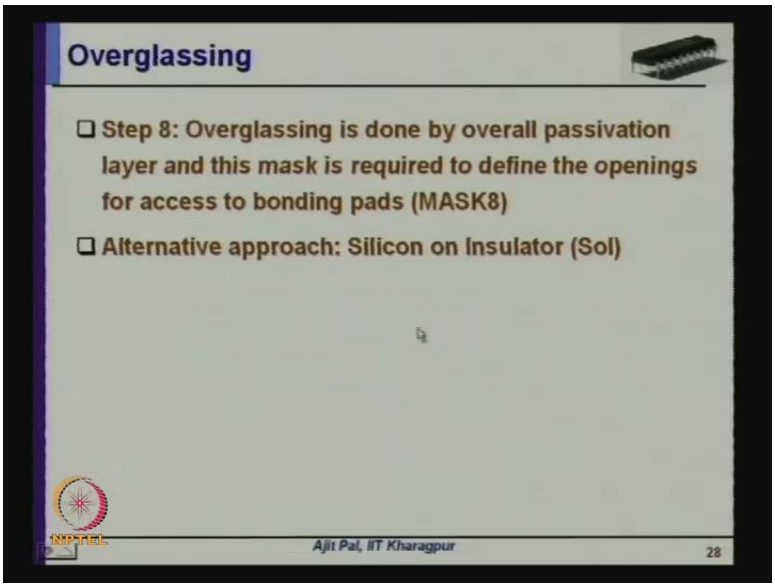

So, you can see this is the MASK 7 for creating the patterned metal layer, another step is also necessary which is known as over glassing. So, over glassing is done by overall passivation layer and then this mask is required to define the openings for access to bonding pads, so once the chip is created you know you have to take interconnections to the outside world then you will have to form a package, so for that purpose you have to again make holes at the appropriate places not only for taking interconnection, but also for the purpose of testing.

So, to test different parts of the circuit you have to you have to make contacts at different points within the chip, so that is done in this step; this over glassing step, so over glassing is done by overall passivation layer and this mask is required to define the openings to access for access to bonding pads, so they will be connected to the bonding pads and then you will form a package either dwelling line package or some other kind of package and then it will be available in the market, before I conclude this part; I think I should tell about another alternative way of realizing CMOS circuits and that approach is known as silicon on insulator.

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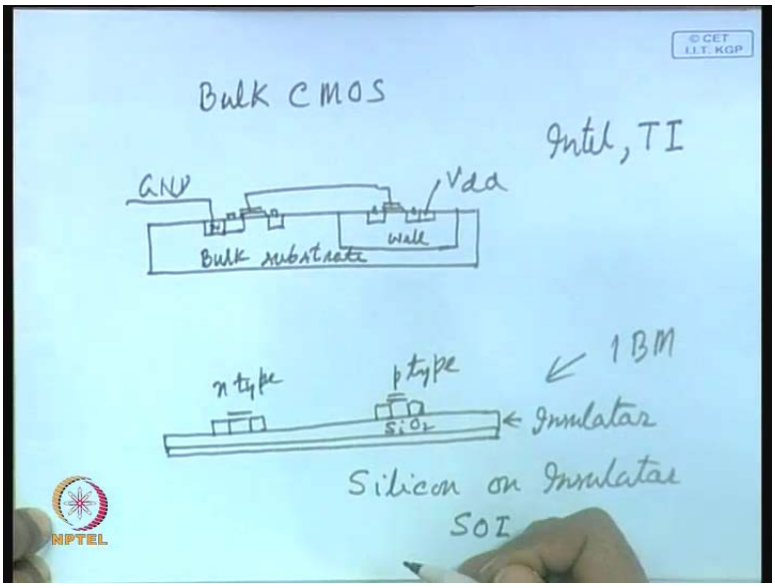

So, here we have seen that in the conventional approach which is also known as bulk CMOS, so here what you are doing you are starting with a substrate and then you are creating the n-well you are creating the nMOS and pMOS, nMOS and pMOS transistors here is the nMOS transistor, here you are creating the pMOS transistors this is the channel region then you are doing the interconnection you are taking you are and you can see this is the you can say this is the bulk you know substrate and in this case, this substrate is entire substrate is connected this is the p plus region is created and this is connected to ground and similarly the entire, you know that this is the well this is connected to v d d this is the bulk CMOS here this is one approach another approach is you will start with the substrate then you will deposit silicon dioxide layer.

So, here is your SOI 2, so this is the insulator and on top of this you will create those various transistors; that mean, you will form a nMOS transistor you will form a pMOS transistor then you will do the interconnections and so on. So, you can see this is called silicon on insulator, this is an insulator and on top of this insulator you are creating different transistors and then of course, you will be doing interconnections among them. So, you can create n type transistor, you can create p type transistor here you are not forming any well, but on a silicon dioxide layer, you are forming different types of transistors and interconnecting them and this is known as silicon on insulator or S O I.

So, there clearly there are two different groups for example, Intel, Texas instruments they are following this approach bulk CMOS approach for realizing VLSI circuits on the other hand the S O I approach is being followed by I B M, I B M is using S O I approach for realizing VLSI circuits and it has been found, that this SOI approach has some good features bulk CMOS also have some good features, so that means, these two approaches have their own advantages and disadvantages particularly SOI approach has been found to be very suitable for low voltage and at low voltage it gives you a very good quality transistors, but it has other problems but that means, all I am trying to tell that this bulk CMOS and SOI these two are two alternative approaches available for the realization of the CMOS, VLSI circuits and some houses are realizing VLSI circuits using bulk CMOS and some houses like I B M they are realizing VLSI circuits by following S O I approach

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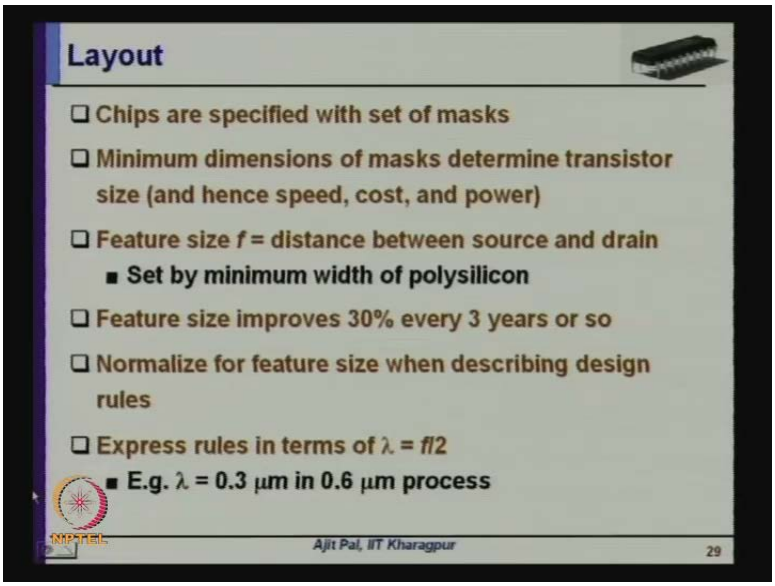

Coming to the last light, you have to make a kind of layout, I have I have simply shown the formation of an inverter, so and I have shown you will require a number of masks to realize the, to create that create different transistors and make the interconnections. So, chips are specified with set of masks you have seen 8 masks, 8 steps are required and 8 masks are required and minimum dimension of masks determine transistor size.

So, they are you know the masks will be created where you have to those are nothing but you know you have to create a kind of a pattern geographic patterns and they will have some separation some you have to maintain some width like that and that will decide the

speed cost and power and a parameter known as feature size f is used which is essentially a distance between source and drain and it is said by the accuracy of the photolithographic technique available on that date and with the improvement of this photographic technique, photolithographic technique this dimensions are getting reduced gradually as you know earlier you had five hundred micron, now you are close to thirty three micron and this is happening because of the advancement of photolithographic and other techniques.

So, this minimum width decides the feature size and feature size improves thirty percent every three years or, so you may have heard Moore's law, so Moore's law tells that every 18 months the number of transistors on a wafer will double how it is happening? The feature size is decreasing and normalize for feature size when describing design rules and whenever you are making the, making the pattern; that means, the layout then you have to follow some design rules, these designs rules are specified in terms of a parameter known as lambda and all these rules are expressed in terms of lambda, lambda is nothing, but this feature size by two; that means, whenever it is a 0.6 micron process then lambda is equal to 0.3 micron.

So that means, the layout is created by following a number of design rules those design rules are specified in terms of lambda that means, the maximum channel length should be two lambda, I mean minimum channel length should be two lambda like that width should be say lambda and those I am not going into the details of those design rules, but they are specified in terms of lambda. So, this is how you will be creating layout and you will realize a complex VLSI circuit.

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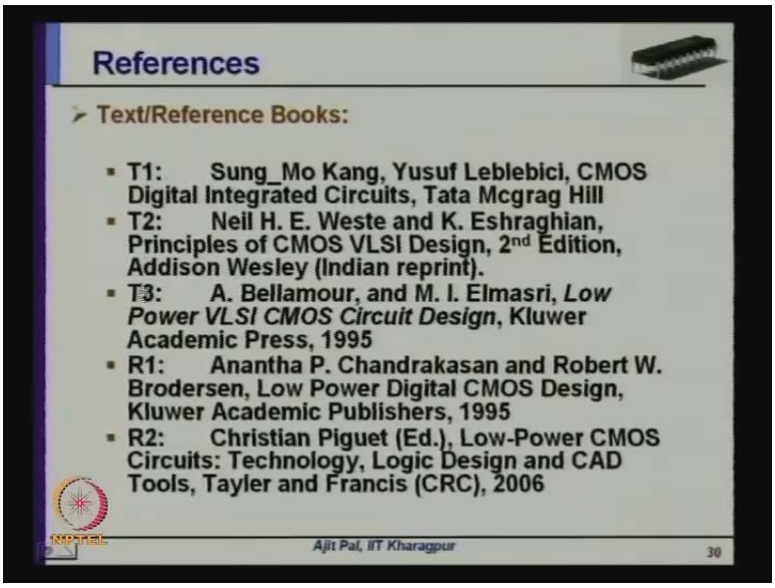

So, with this you have discussed to summarize what we have discussed today we have discussed the structure of MOS transistors and you have seen there are four different types of transistors possible in MOS, nMOS enhancement type, nMOS depletion type pMOS enhancement type and pMOS, pMOS enhancement type and pMOS depletion type and you can use them realize circuits different types of functional circuits like inverter NAND gate, NOR gate and other things then we have discussed the fabrication steps, particularly fabrication steps of a CMOS circuit and we have seen there are two basic approaches that is one is your one is based on that traditional approach bulk CMOS another is your silicon on insulator approach.

Now, I would like to give you some references, so this first book by Kang, Kang CMOS digital integrated circuit, this book gives you the background material that will be required for the scores it discusses in details of CMOS circuits starting with MOS transistor, MOS invertors, MOS complicated circuits similarly waste and Eshraghian's books also gives you necessary background for CMOS circuits, then coming to low power circuits this book is very good by bell amour and Elmasri, low power VLSI CMOS circuits, but unfortunately as you can see this book was written in 1995, it is little old and another book is also there by Ananth P Chandrakasan and Robert W Brodersen low power digital CMOS circuit design published by Kluwer academic that also published in 1995. So, these two books are primarily on lower power CMOS circuit design, but unfortunately these are not available in Indian edition.

So, I requested the library to purchase few copies of these books these books may be available in the library another recent book is a edited version edited by Christian Piguet and low power CMOS circuits technology logic design and CAD tools this is a more recent book. However, you will see that major part of my lectures particularly in the latter part will be based on material taken from papers, I cannot really give you any I mean copies of everything, but later on I shall provide you some of these papers, copies of some of these papers. And lecture notes are also available, but it may not be necessary for you, because these lectures will be uploaded in the in our CUT website.

So, you can access them may be after one or two days, and you can go through them again and again if necessary. So, with this we have come to the end of today's lecture, in the next lecture we shall discuss about a model by which you can explain the operation of pMOS transistors that is known as Freud model that we shall discuss in the next class. Thank you very much.