Low Power VLSI Circuits and Systems

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Lecture No # 01

Introduction and Course Outline

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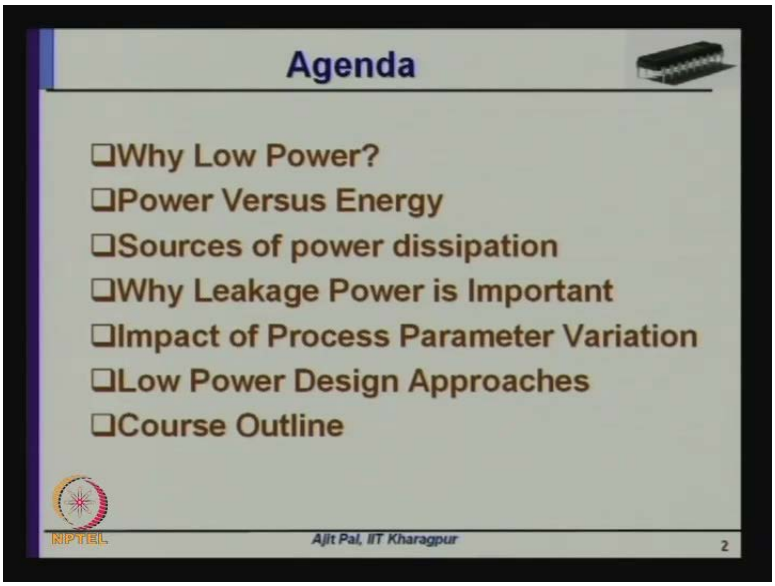

Hello, and welcome to this course on low-power VLSI circuits and system. This is the first lecture of this course; topic is introduction and course outline. And here is the agenda of this lecture. First I shall discuss why low-power why low-power is so important in the present day context, then I shall discuss two terms power and energy and what are the differences, which one is important in which context a particular parameter is important, then I shall discuss various sources of power dissipation. So, whenever you are fighting an enemy you should know their; you know that their limitations their weaknesses so that you can fight them. So, these sources of power dissipation will identify their show their limitations and diffidence of power dissipation on various parameters.

So, once we identify those parameters it will be very useful to reduce power dissipation by controlling those parameters. Then I shall discuss about leakage power and in particularly why leakage power is becoming more and more important in the present day context. Earlier leakage power was not very important, but in the present day context it is becoming very very important and why it is important that I shall discuss, and after that I shall discuss about impact of process parameter variation. What is happening, as the device dimension is getting reduced we are as we are going to deep submicron technology the you know the variations are becoming very important, and as a consequence various parameters like channel and threshold voltage these are no longer constant. So, they vary over a range and there is a, you know you have to take into account that variation. So, what is the impact of process parameter variation that we shall briefly discuss, then I shall mention about low-power design approaches, what are the different approaches that has to be done for reducing power dissipation and finally, I shall give a course outline.

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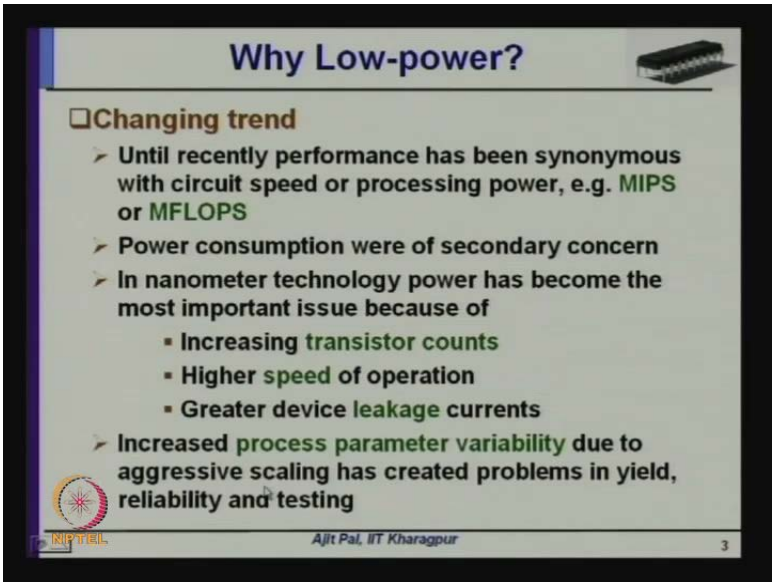

So, let me now focus on why low-power first thing first important requirement is the changing trend as you can see, until recently performance has been synonymous with circuit speed or processing power expressed in terms of MIPS or mega FLOPS. So, whenever the particular processor spec people are telling what are the specification people will say it runs on. So, many mega FLOPS; that means, So, many millions of floating points operations it can do or MIPS millions of instructions it can execute, but

now the situation is changing you have to you know earlier power consumption were of secondary concern; that means, people were more concerned about improving the performance rather than looking at the power consumption. So, power consumption were of secondary concern; however, in nanometer technology which we also called deep submicron technology power has become most important issue because of several factors number one is increasing transistor count as you know as the device dimension is getting reduced you are able to put more and more transistors on a chip and as a consequence power dissipation in increasing and power density is increasing and you have to give more attention to power, than higher speed of operations as you know in the early years of microprocessors the microprocessors used to operate in the kilo megahertz range 3 megahertz 5 megahertz 2 megahertz and so on. But now all the processors are operating in the gigahertz range. So, speed of operation has increased and you will see later on the power dissipation is directly related to speed of operation, rather power dissipation is the is proportionate to the frequency of operation of the processor. So, as the frequency of operation is increasing you are getting higher speed of operation the power dissipation is increasing and you have to give more attention to power. And then later device leakage current, you know in the early years may be up to 100 nanometer leakage power was of no concern, leakage power or the static power dissipation was very small, but that is no longer true in say 33 nanometer or 66 nanometer and as a consequence you have to give more attention to leakage power and you have to develop techniques by which the leakage power can be reduced.

And another important factor which is also becoming predominant that is increased process parameter variability, due to aggressive scaling as you know there is aggressive scaling is taking place from early years of 500 nanometer we have come down to 45 nanometer 65 nanometer very soon 33 nanometer devices will be used to fabricate microprocessors and when you do that it is creating problems in yield because, of processed parameter variation various parameters as I told those channel length threshold voltage and those important parameters which affect the performance of the device is no longer constant. So, those variations are affecting the yield and; obviously, yield is getting reduced as you are doing aggressive scaling and not only yield reliability is getting reduced because, chip is becoming more vulnerable to failure and it is becoming also very difficult to do the testing. So, yield reliability and testing these three are creating problems as you are going to deep submicron technology.

So, what the way out only way is out is to go for low power you have to develop chips which consumes lesser and lesser power. So, that is one of the most important reasons for considering low power in the present day VLSI design context.

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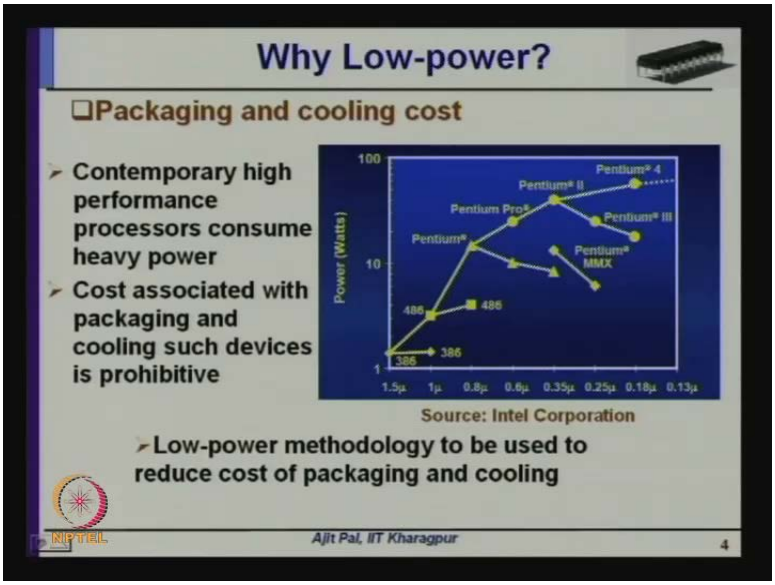

Then packaging and cooling cost, as you know the packaging and cooling cost is dependent on the power dissipation of the chip. So, you have to take out the heat from the core of the chip, otherwise it will start malfunctioning and this packaging and cooling cost is increasing and as you can see contemporary high performance processors are consuming more and more power. So, you can see here that 3 8 6 processor used to consume only say 1 or 2 2 to 3 watts of power. Now as you are as you are going for more high performance processor like Pentium, you can see it has reached about 100 watts. So, whenever a processor is dissipating 100 watts you have to develop suitable packaging and cooling technique, you may be I do not know whether you have opened any BC you will find that inside the BC on top of the processor there is a big heat sink and not only that there is a fan. So, packaging and cooling is becoming very very important and unless you are able to reduce power dissipation the packaging and cooling cost will keep on increasing. So, cost associated with packaging and cooling such devices is prohibitive. So, it is important to develop low-power methodology to reduce the cost of packaging and cooling; obviously, as you know Moore's law tells that the cost also will fall. So, cost will fall only when the cost of packaging and cooling reduces.

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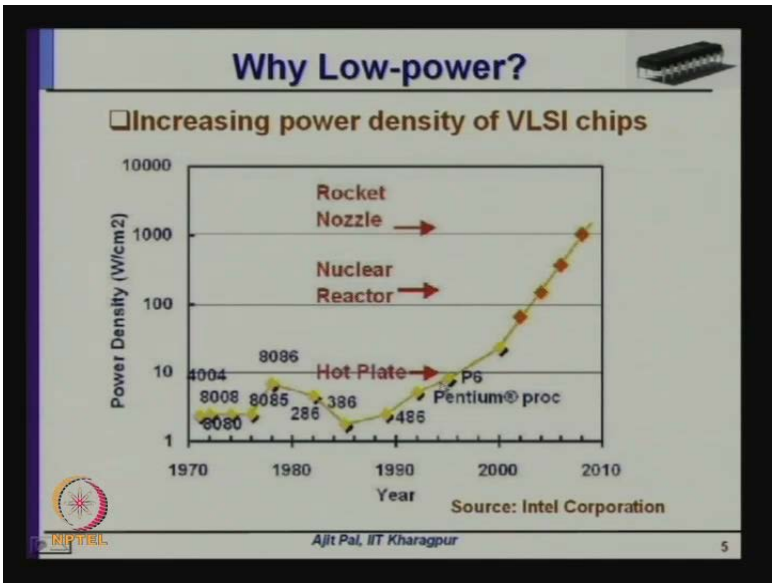

So, low-power methodology is very important to achieve this goal. Then comes the increasing power density, as I was telling then as you have putting more and more transistors on a single chip the as the device dimensions have becoming smaller and smaller the power density is increasing that is watt per centimeter square. So, that is increasing and as you can see starting from 8080 to various chips the chip is becoming. So, hot it is irony the power density is very closed to hot plate; hot plate is used for cooking. So, you know there is a joke may be there was a joke that there is a cyber cafe where, you know can not only check your emails, but you can order for omelet and omelet will be fired by putting beef the putting the you know that where container on the chip it will be so hot as anyway. So, we do not we cannot allow this. So, you have to reduce the power density by applying suitable low-power technique. So, that it does not really go beyond this. Finally,

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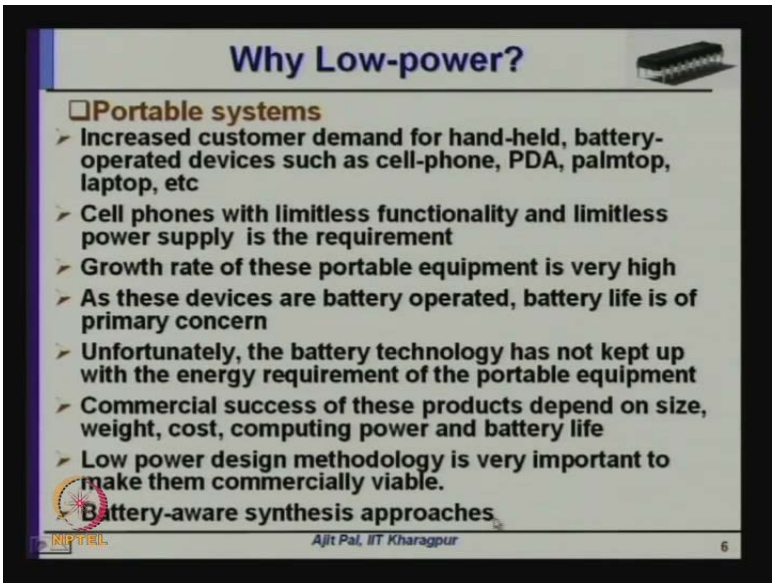

Finally, you know the number of portable systems is increasing at a very high rate, and there is a increased customer demand for hand held battery operated devices as like cell phone, PDA, palmtop, laptop etcetera. And you know not only that not only there is a high proliferation of portable handheld devices their functionality is increasing earlier as you know cells phones were commonly used for talking, but now what is not in cell phone. So, everything is you are demanding everything from a cell phone. So, cell phones with limitless functionality and limitless power supply is the requirement because, whenever you provide limitless functionality your power consumption will increase, as you put more and more functions in a cell phone like camera then internet access then voice recording FM radio and so on. It is power consumption will keep on increasing.

Unfortunately as I told, but may be fortunately growth rate of this portable equipment is very high, compared to you know desktops or servers you know the number of such portable devices like cell phones, PDA,s laptop, palmtops is increasing at a very high rate, and growth of this growth rate is very high, But unfortunately all these devices are battery operated and battery life is becoming is of primary concern and unfortunately the battery technology has not kept off with the energy requirement of the portable equipment. You will see that the power consumption is increasing at this rate, there is the power consumption of the devices or systems and may be battery technology is increasing improving at this rate. So, over the years so this is the battery technology. And

as you can see over the years the gap is increasing. So, the power consumption versus the battery technology; that means, the capability of battery power density of battery is definitely improving over the years, but power consumption is increasing at at a much faster rate and this gap is increasing.

So, commercial success of these products is dependent on size, weight, cost and computing power and battery life. So, whenever you go for selecting a cell phone what you will look for how long the battery will sustain or whenever you go for purchasing a laptop, you will see that without charging it will you can operate it for may be the twelve hours or may be whole day. So, commercial success of these products heavily depends on size, weight, cost computing power and battery life. Obviously, size is dependent primarily on the battery size you will see that in most of the portable equipment battery size is dictating the size of the device because, that is the that is of being that is the most important component and its size is maximum. So, low-power design methodology is very important to make them commercially viable.

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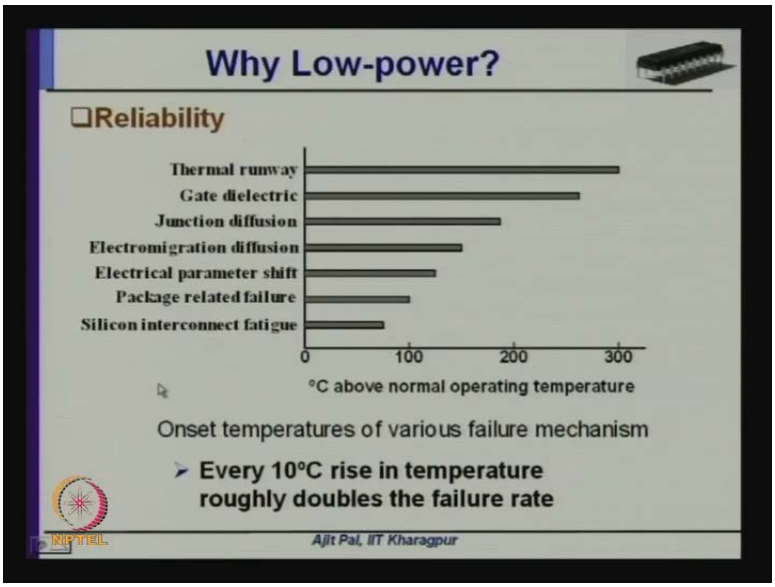

Finally, reliability as I was telling reliability is very important in VLSI chips, and as you can see as the power consumption is increasing temperature will keep on increasing unless you provide proper heat sink to dissipate the power. And you can see there are various failure mechanisms like thermal runaway, gate dielectric, junction diffusion, electro migration diffusion, electrical parameter shift, package related failure, silicones

interconnect fatigue these problems will keep on arising as the temperature increases. And it has been found that, every 10 degree centigrade rise in temperature roughly doubles the failure rate. So, what is the conclusion to make the chip reliable it is very important to use low-power design methodology. So, that power consumption is small rise in temperature is small, beside the chip can operate at a very at an unreliably. So, from the reliability point of view low-power design methodology is extremely important.

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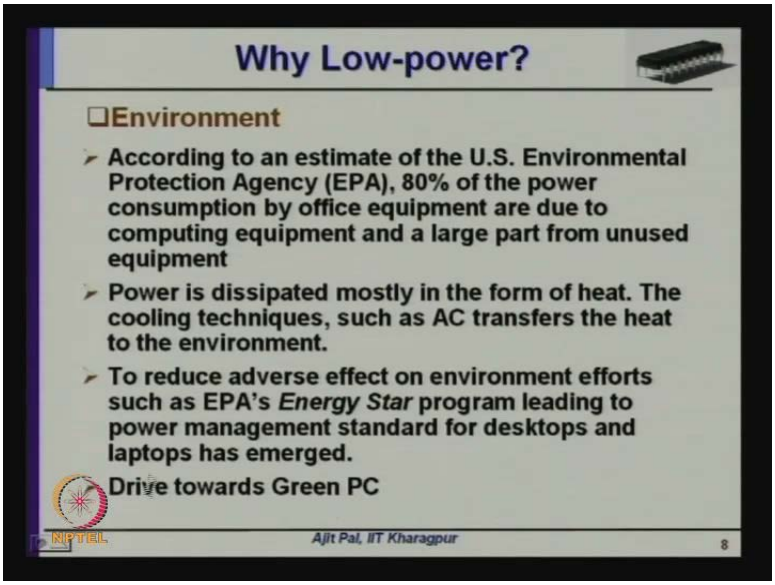

Finally, impact on environment U.S. environmental protection agency, it has been it has been found that 80 percent of the power consumption by office equipment are due to computing equipment; that means, computers and printers and other related devices and a large part from unused equipment. This is that means, if you visit some offices you will find that computers and other symptoms are on, but they may not be used, but still they are on. So, those unused equipment also consume lot of power. And In fact, whenever this power is dissipated and mostly in the form of heat, and what you normally do you have to use some cooling technique such as air conditioner to transfer the heat to the environment so; that means, the heat that is being released by these computing equipment is released ultimately released to the environment.

So, it has impact on the environment and to reduce adverse effect on environment effort such as those EPA'S environmental protection agents agency is star energy star program leading to power management standard for desktops and laptops have has emerged you

know now a day's situation is little different. So, whenever you are not using a desktop or a laptop you will find automatically screen is becoming blank and the power hungry components are automatically shut down by the power management circuit. So, that is actually result of this you know the standard power management standard for desktops and laptops. So, this concern about environment has lead to drive towards green p c and; obviously, this consciousness about environment also dictating low-power design methodology you have to use low-power design methodology. So, that environment is not affected. So, I believe even now fully motivated about these require mental low-power methodology you see there are.

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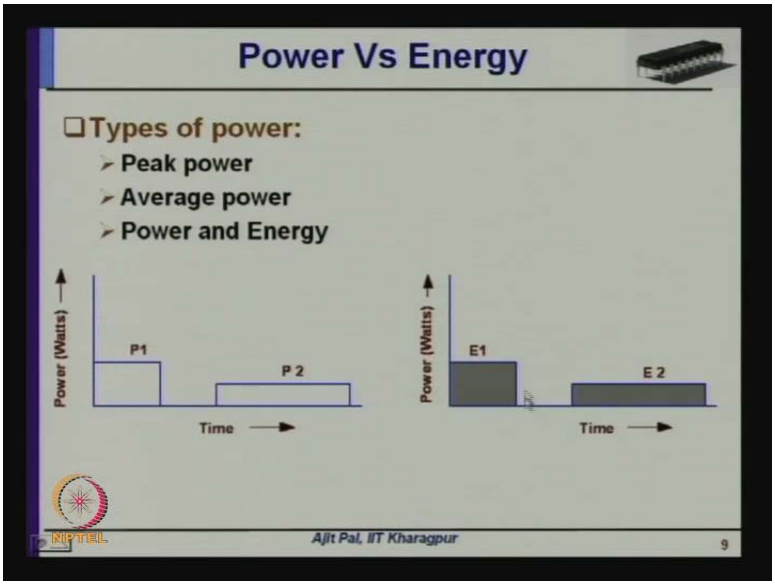

So, many reasons for low-power methodology now let us now focus about low I mean about some of the technical things whenever we say power or low-power what do you really mean there are three types of power dissipation one is peak power what is peak power peak power is essentially say suppose, you plot the power dissipation over time.

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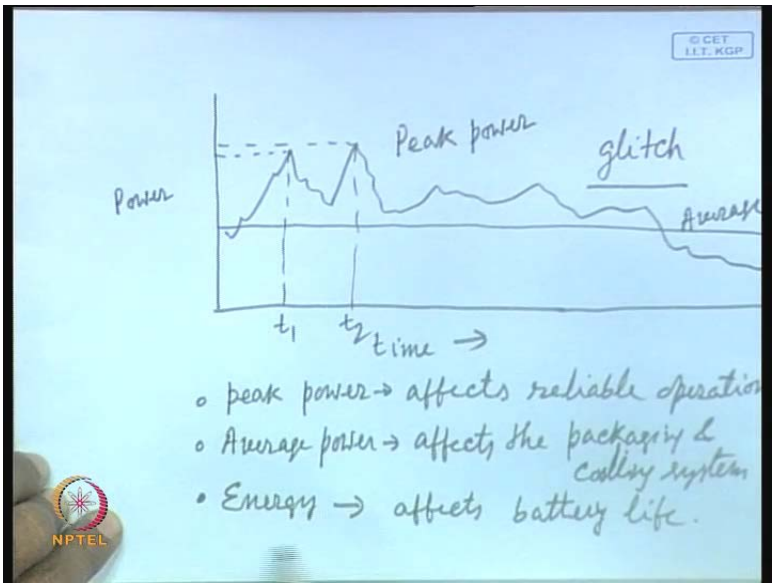

So, this your power dissipation you will find that it is not really constant, depending on the application you are running some time the power consumption is high, sometime it is low some time it is may be very low like that. So, the power dissipation varies over time and you can see there are some points where it is drawing very heavy power and this is your peak power. So, peak power is the maximum instantaneous power at a particular time may be t 1 and here at time t 2. So, peak power is the maximum instantaneous power. What it really affects it affects the reliability of the upper reliability of operation of the system because, whenever this kind of heavy current is drawn this current will flow through the power line; that means, the power supply will has to deliver power through the power line to the chip or the VLSI circuit, and there will be it has some finite resistance and as a consequence some there will be some voltage drop in that power line and that will lead to what is known as glitch on the power line and glitch on the power line may lead to malfunctioning of the chip and unbelievable operation of the devise.

So, peak power essentially affects, peak power affects reliable operation. This is one type of power, second is your average power average power what does it affect. So, this is the peak power that mean, how the power varies over time if you take average may it will be somewhat like this is the average power. This average power affects the packaging and cooling system, packaging and cooling system. So, packaging and cooling is affected by the average power; that means, if the average power is high you have to you have to develop suitable packaging and cooling. So, that the heat is taken out from the chip, third

one is energy what do you really mean, by energy in a power is the rate of rate at which energy is drawn from the system may be from battery or from the power supply. So, the rate at which energy is drawn from the power source is the power dissipation. So, in the context of battery operated systems that mean, it affects battery life energy affects battery life let me explain with the help of this diagram here, as you can see during the operation of a processor over time you can see this is the average power dissipation p 1.

So, p 1 is the average power dissipation accordingly the packaging and cooling system has to be designed and here the average power dissipation is p 2. So, this line so this is this is expressed in terms of watt now what is energy is the area of this; that means, power dissipation and this is the time you have to multiply the time with the power dissipation to get the energy drawn from the power source may be battery in portable systems; obviously, this will be from the battery.

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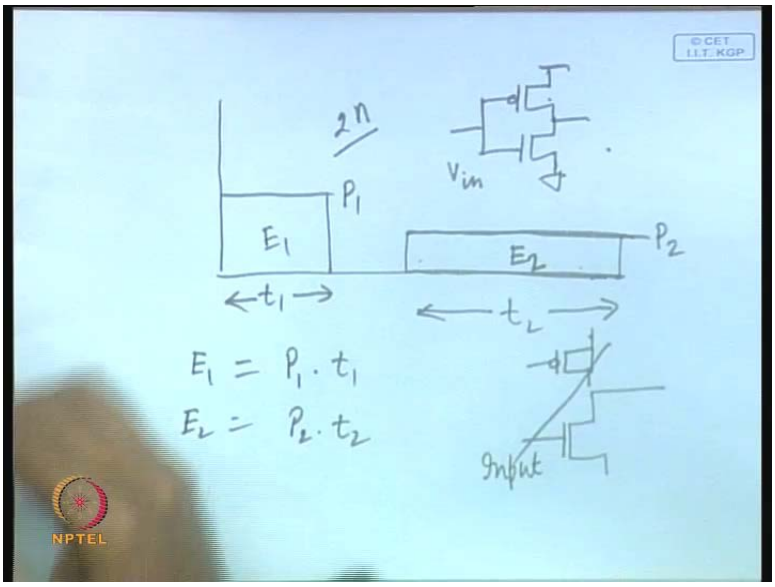

That means, if the if this is let me draw this curve once again say this is the p1, and let us assume this is time t 1. So, energy E 1 is equal to p 1 into t 1, now let us assume the here it is. So, this is your t 2 t 2 is double that of t 1 and power dissipation is also half. So, here you can see E 1 this E 1 is equal to p 1 into t 1 and here E 2 is equal to p 2 into t 2. So, power average power dissipation is half, but the duration is longer. So, here you can see E 1 and E 2 these two are same, but the power dissipation is different. So, what can happen sometimes you can reduce the power dissipation by slowing down the clock

frequency, but again that will increase the computation time. So, energy drawn from the power source may remain same, but in the context of battery operated system this energy is most important parameter and usually it is expressed in terms of power into delay power delay product.

So, sometimes power and energy these two terms are used interchangeably although these two are different particularly in the low-power context low-power design methodology context when you are considering the battery operated systems there actually the energy is the most important thing. So, sometimes we will tell power, but actually you are trying to tell energy. So, when we say low power essentially it is low energy. So, it is very essential to understand the difference between power and energy is it clear.

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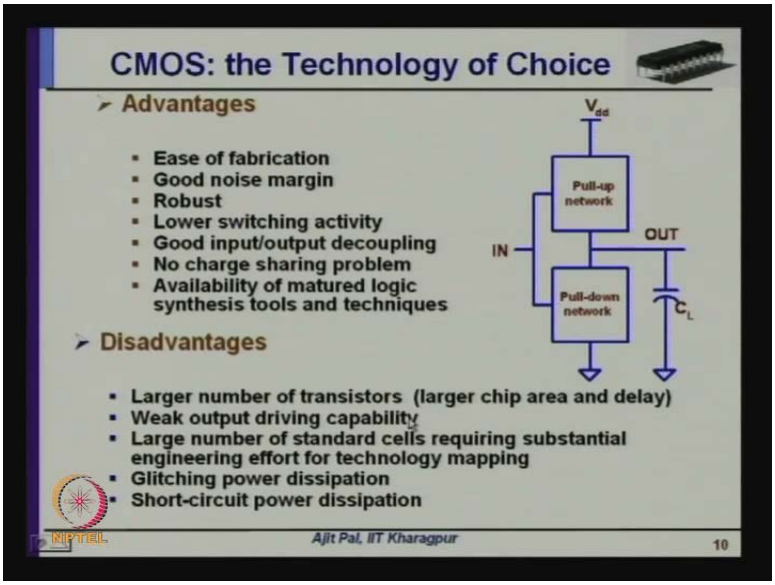

Now, let us consider the technology that we shall be using. As you know there are various technologies which have been used for the fabrication of I g we are not considering the early systems like TTL transistor logic or PMOS or NMOS which were used earlier, but in the present in the context CMOS is the technology of choice. CMOS is used for fabrication of all the VLSI chips now a days, and this the basic structure of a CMOS circuit, you have a pull-up network or PMOS transistors I shall discuss in detail later on and here you have got pull-down network or NMOS transistors and here is the input which are going to the gates and the output is taken from the junction of PMOS

network and NMOS network and this is the output. And you know that there is a load capacitance given the SCL now you may be asking why CMOS is the technology of the choice because, of it is various advantages what are the advantages number one is ease of fabrication the fabrication technique has been standardized matured and now it is very reliable; that means, CMOS fabrication technology has matured and it has become very reliable over the years. Then it has got good noise margin later on I shall discuss in detail CMOS provides you better noise margin compared to other stripes of circuits like NMOS or PMOS or TTL and it is very robust by robust means, under different hazardous condition like when there is change in supply voltage when a little bit of change in supply voltage, there is noise under that circumstances it will operate reliably CMOS circuits are no robust.

Then lower switching activity later on we shall see the switching activities lower in CMOS circuits particularly in static CMOS circuits, then good input output decoupling this good input output decoupling arises because, in CMOS circuits you will see that input is applied to the gate. So, you are applying input to the gate of a single transistor or a network of transistors and you are taking output from the may be from let me draw once again.

So, this is a PMOS transistor this is NMOS transistor. So, I have drawn very simple invertors. So, you will be applying input to the gates and taking output from the you can see from the junction of the source and drain, and since this input is of very high impedance because, of silicone dioxide present here and here there is a good input output decoupling in CMOS circuits. And later on we shall discuss about charge sharing problem and you will see in CMOS circuit there is no charge sharing problem compared to other techniques, like dynamic CMOS and other things and as I mentioned there is availability of matured logic synthesis tools and techniques, which are available cad tools are available which can be used to synthesize CMOS circuits and because, of these advantages CMOS is the technology of choice of course, in this world nothing is one-sided there are some disadvantages and difficulties which are listed here, you have got large number of transistors because, you are using as you can see two transistors although one transistor may serve the purpose to realize the same functionality you are using two transistors as a result number of if you have got n input here n is equal to one you have got two transistor similar, if there are n inputs you will require 2 n transistors.

So, as a consequence area is larger and delay is longer. So, because of this duplication of the transistors in the realization of CMOS circuits the chip area is larger and delay is longer and weak output driving capability you will see when whenever you are realizing a complex circuit a the output is taken through a chain of NMOS and PMOS network and as a consequence resistance is high and driving capability is poor. Large number of standard cells required substantial engineering effort for technology mapping, you will see whenever you realize a very complex circuit you have to use different types of standard cells like inverter 2 input and gate, 3 input nand gate, 4 input nand gate, 5 input nand gate, 2 input nor gate, 3 input nor gate, 4 input nor gate and so on. So, then different types of flip-flops and so on.

So, you require a large number of standard cells and whenever you realize circuit and that step is known as technology mapping you have to select different cells to realize circuit. So, that requirement is there and later on we shall see there is glitching power dissipation in CMOS circuits because, of the delay as I mentioned there is a delay large delay in CMOS circuits and that has led to glitching power dissipation, and also there is short circuit power dissipation which I shall briefly discuss shortly.

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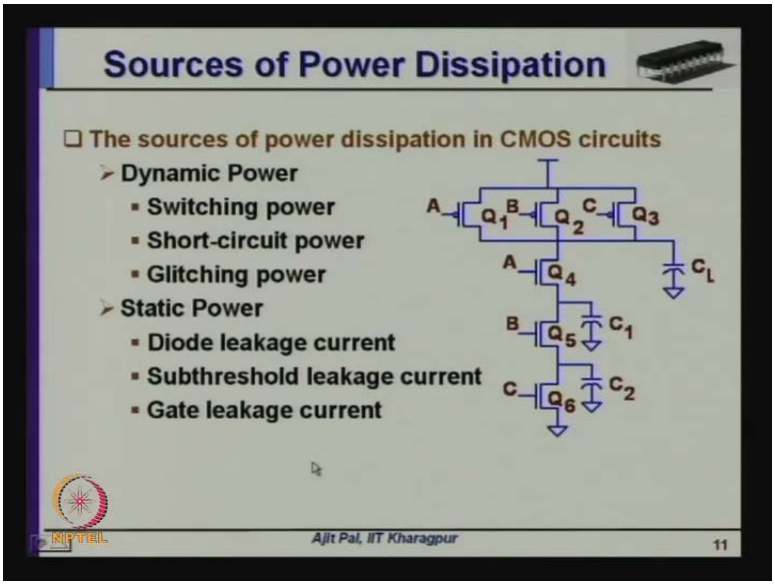

So, now comes the sources of power dissipation this is a typical CMOS circuit 2 import nand gate, I have shown 3 input nand gate, I have shown you can see it has got associated with a large number of parasitic capacitances. This is the load capacitance c l

a part from that there are other capacitance c 1 at this junction, c 2 at this junction. So, there are large numbers of parasitic capacitances which are present inside the circuit and the sources of power dissipation in CMOS circuits can be broadly divided into two types' dynamic power and static power. So, dynamic power is essentially when the circuit is in active condition when the circuit is in use when you are changing the input when there is a clock present in the circuit that time whatever power dissipation take place we call it dynamic power dissipation.

On the other hand whenever the circuit is in standby mode circuit is not in use it has been it has been kept in the standby mode as I was telling when the circuit is not used that part of circuit is shut off shut off means, you are not applying not changing the inputs you are not applying the clocks and, but unfortunately there will be some power dissipation even in that standby condition primarily because, of various leakage currents. And leakage currents can be broadly divided into three types diode leakage current sub threshold leakage current, and gate leakage current similarly, the dynamic power can be divided into three different types switching power short-circuit power and glitching power

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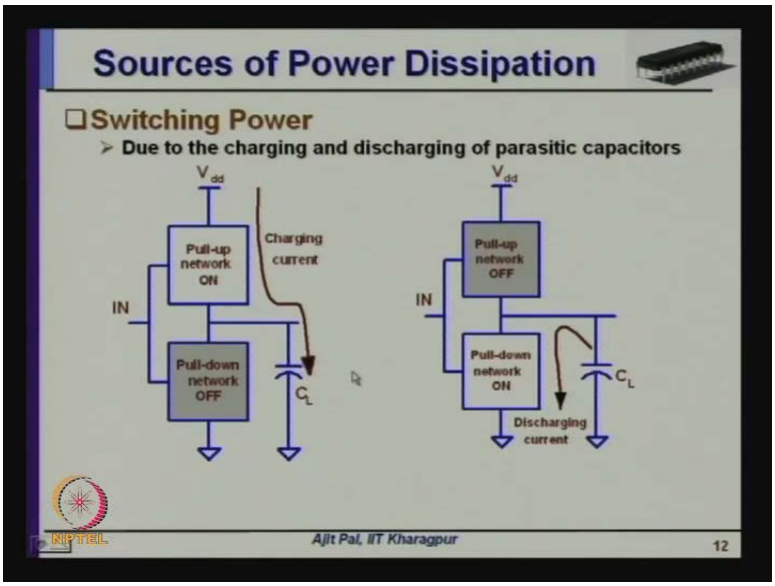

Let me very briefly discussed about these this sources of power dissipation switching power switching power is the most predominant component of power dissipation in c m o s circuits, and particularly this happens when the circuit is in dynamic mode. So, when the circuit is in dynamic mode this power dissipation occurs. So, this switching power

dissipation occurs due to charging and discharging of current. Charging and discharging of current leads to power dissipation as I have told it has got associated with some parasitic capacitances, when the output is becoming high; that means, you have applied some input combination such that output is high that time this load capacitor c l will charge from the source through this NMOS PMOS network pull-up network and as it charges some power will be dissipated in this pull-up network because, of it is you know resistance and similarly, when the output becomes 0 the charge which is accumulated in this capacitor when it was one I mean, output was high or one that that will get discharged through this pull-down PMOS transistor NMOS transistor network here there is NMOS transistor network.

So, pull-down NMOS transistor network it will get discharged and again power will be dissipated in this NMOS transistor network because, of their finite resistances. So, the switching power dissipation is primarily due to charging and discharging of parasitic capacitances. And this power dissipation will dependent on the supply voltage load capacitance and other activities switching activity the rate at which the transitions occur and so on. Later on we shall discuss about it in more details.

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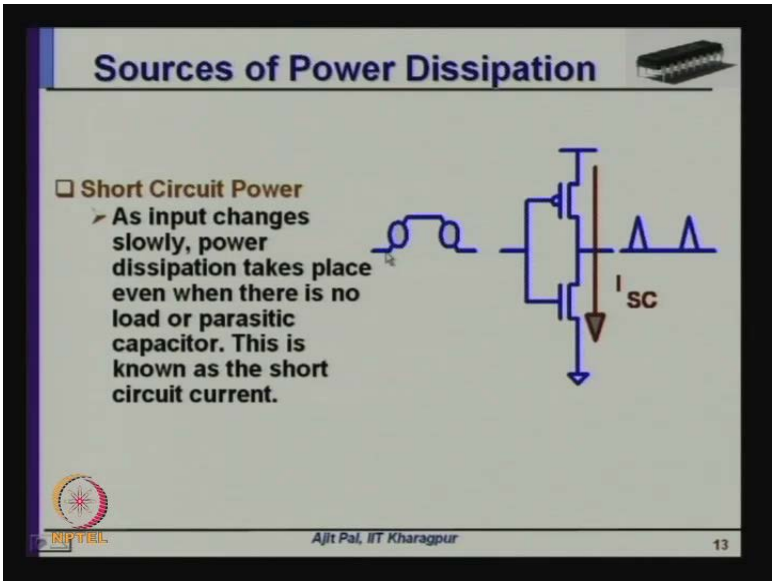

Then comes the short-circuit power, short-circuit power dissipation occurs because of slowly I mean, slow change of the inputs as you can see here input is changing in ACMO circuit as the input changes slowly like this say.

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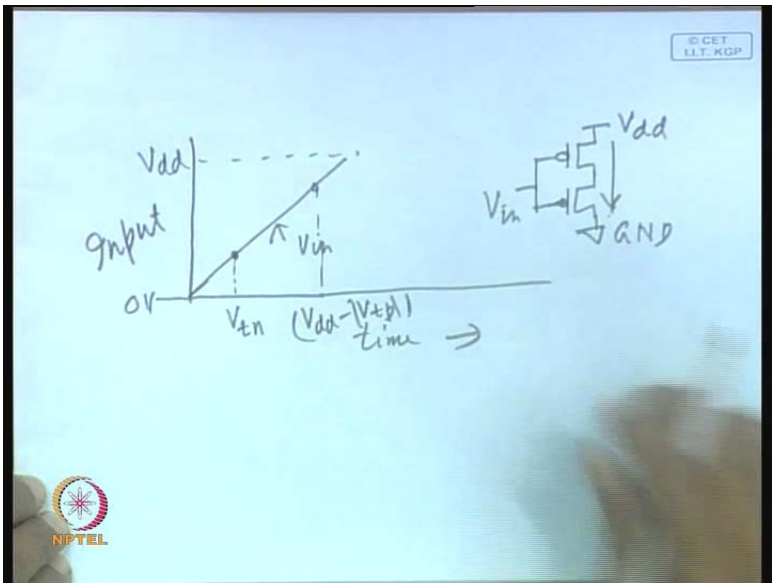

I have drawn it in a little exaggerated form this is time and this is input voltages changing and let us assume this your v d d and this is 0 volt and here it is time and let us assume this is a inverter simple circuit inverter. So, you have got a PMOS pull-up network and NMOS pull-down network and here you have applied this v input this is your v in. So, this is applied to this. So, initially as the input is increasing you can see this voltage is less than threshold voltage of this transistor and at that time this transistor is off this transistor is also off, but as the input voltage increases and as it reaches the threshold voltage of the NMOS transistor then this transistor will turn on and this transistor will turn on and as you know during that period this was already on; that means, during this period only PMOS transistor is on, but here from this because input is 0 and so, there is a be with this voltage gate voltage is gate to source voltage is such that this transistor is on even for during this period, but this was off.

So, there was no current flow, but from this point onwards both the transistors are on and it will continue till you reach v d d minus v t p. So, for this during both the transistors is on as a result current inflow through this path as if the v d d is sorted to ground, and this is known as short-circuit power dissipation. So, short-circuit power dissipation primarily arises because, of slow change of inputs. So, power dissipation take place even when there is no load or parasitic capacitor; that means, even when there is no capacitance here this power dissipation will take place because, the supply voltage is sorted to ground through this PMOS and NMOS transistor and it may not be an inverter it may be a

complex circuit in such a case this will be a complex PMOS network and this be may be a complex NMOS network. But there will be a current path through the circuit when the input is greater than v t n and less than v d d minus v t p. and this current this power dissipation is known as short-circuit current short circuit power dissipation.

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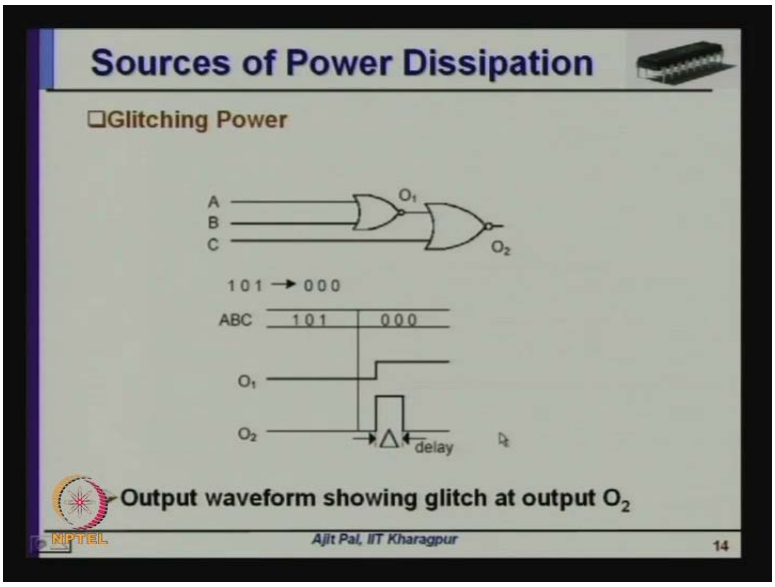

Finally, the another the third source of dynamic power or dissipation is glitching power this glitching power dissipation occurs due to due to delay finite delay of the gates for example, here you have got a got two nor gates a and b is applied to this gate output is q 1 and this q 1 and c is applied to the second nor gate normally whenever the input is 101 what should be the output at q 2 it should be 0 similarly, when the input is 000; that means, A 0 B 0 C 0 output again will be 0, but you can see here when the input is 101 this output is 0 this output is 0. And it will change to one this 0 will continue for certain during because, of this delay when this what whenever it becomes 000 this output will become 1 and this 0 will is responsible for this high output for a very small duration that means, this input whenever the input is changing from 101 to 000 because, of the finite delay of these gates there is a one the output is becoming high for a very small duration and this is known as glitch. So, glitch is generated at the output because, of finite delay and as you know there is a capacitance present here and there will be power dissipation in that capacitance. So, there will be glitching power dissipation on this output capacitance.

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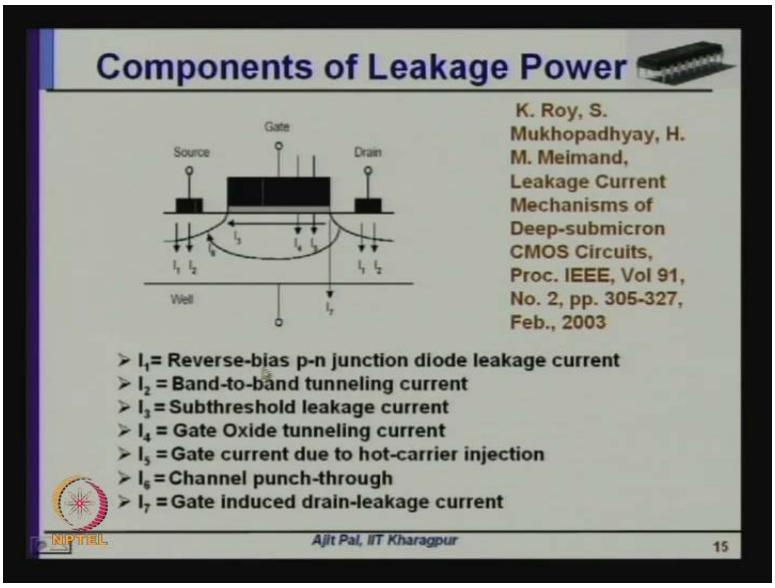

So, this leads to glitching power dissipation because, of finite delay of the gates. Then coming to the static power dissipation that is your leakage power, you can see here a simple MOS transistor is shown this is a source is drain this is the gate structure and different types of leakage currents are listed here, and this is taken from a paper by Kaushik Roy and his group and here is the different leakage currents. I1 reverse-bias p-n junction diode current. So, this you have bought here junctions because, this is this is a this is a PMOS NMOS transistor this will be n plus and this will be p type substrate. So, there is a junction here similarly here there is a junction this is n plus and this is p type substrate. So, in these junctions the junctions or these diodes it is forming some kind of diode and those diodes will be reverse-bias during normal mode of operation as you know when a diode is reverse-bias there is some leakage current there is some reverse-bias current. So, there will be reserve-bias p-n junction diode leakage current later on I shall discuss about it in more detail and particularly although this current is small, but when the number of transistors is millions then total leakage current can be substantial.

Then band-to-band tunneling current that occurs in these junctions the electrons will go from valence band to conduction band because of high energy acquired high electric field present and that leads to band-to-band tunneling current. Later on you and I shall discuss about in more detail then third type of a leakage current I see that flows through this channel is known as sub threshold leakage current normally we know that whenever the gate voltage is less than the threshold voltage v t this transistor is off no current flows

through the channel, but ideally this is not true, even when the gate voltage is little more than 0 some channel current is flowing and particularly the input voltage is very close to v t v t n and little less than that than the leakage current is this has sub threshold leakage current this current is very high and this is known as sub threshold leakage current because, input voltage is less than the threshold voltage even then there will be current flow through this channel.

So, this sub threshold leakage current is substantial in transistors of smaller dimension in particularly in deep submicron technology then gate oxide tunneling current as you know as the device size is shrinking the size of the thickness of the gate oxide is becoming smaller and smaller. It is becoming so thin that it is a layer of few molecules may be two to or three molecules of silicon dioxide and what happens the electrons particularly electrons they acquire. So, much energy that they that silicon dioxide layer leading to what is known as gate oxide tunneling current. So, gate oxide tunneling current is flowing between gate and the substrate I four then gate current due to hot hot-carrier injection hot-carrier injection is due to you know that because, of heavy electric field electrons acquire. So, much of energy they are termed as hot electron. So, and although hot holes are also possible, but they because of their mass heavy mass they do not constitute they do not contribute much for this current, particularly electrons are responsible for this hot-carrier injection current. So, those also flow through this silicon dioxide. Then channel-punch-through occurs because you know as the dimensions are getting reduced this you know this particular source and drain is becoming very close and their pinch of regions are becoming too close and they may touch leading to what is known as channel punch-through and as a result current will flow through the channel between source and drain. This is again a power source of power dissipation finally, gate induced drain-leakage voltage. So, particularly when the supply voltages are I mean, large drain voltage is large and whenever gate voltage is large that leads to what is known as g I d l current great gate induced drain-leakage current and this gate induced drain-leakage current is becoming if more and more predominant in deep submicron technology. So, these are the various sources of leakage power I shall discuss about them in more details later on.

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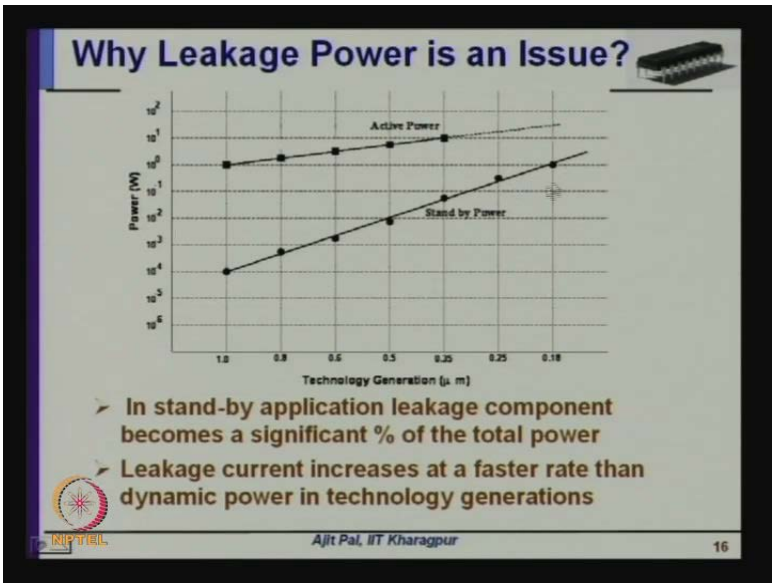

Now, coming to leakage power it is becoming more important because, as you can see the active power is increasing. As we are going from one technology generation to next technology generation as the device size is becoming smaller and smaller, but the leakage power which is represented by standby power is increasing at a at a much higher rate, and leakage current is increases at a faster rate than dynamic power in various technology generations and as a consequence you can see at a at some point this the leakage power will be more than the active power.

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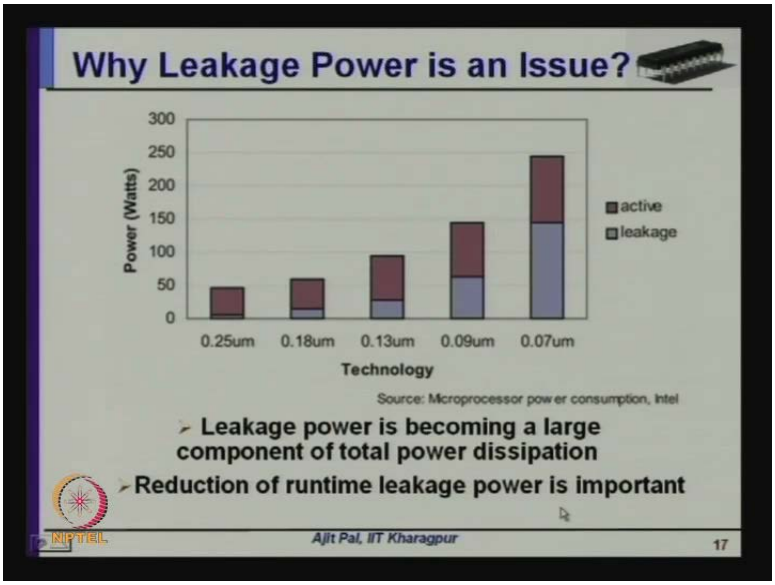

As it has happened here for example, up for point to find micron technology the leakage power is very small compared to dynamic power dynamic power is more predominant, but as you are going from say 0.25 micron, to 0.18 micron, to 0.13 micron as you can see the leakage power component is increasing. And whenever it is 0.07 micron that is your 17 nanometer you can see the leakage power component is more than the dynamic power or active power. So, in the present context particularly discussing about deep submicron technology circuits to be realized by using deep submicron technology using 45 nanometer or 33 nanometer technology there the leakage current leakage power dissipation will be more than the dynamic power and. So, you have to give more attention to the reduction of leakage power and another important factor is reduction of runtime leakage power is important earlier you know this leakage power was very small compared to dynamic power; that means, when the circuit was in standby mode then power dissipation was considered to be very small only during runtime the dynamic power was considered to be important, but as leakage power is becoming more and more during runtime you have to also consider the leakage power component in addition to the dynamic power. So, runtime leakage power is becoming important earlier the leakage power during standby was important. So, people used to reduce the leakage power only during standby mode how to reduce leakage power during standby mode, but now you have to focus on the reduction of leakage power even when the circuit is in active mode or circuit is in runtime condition.

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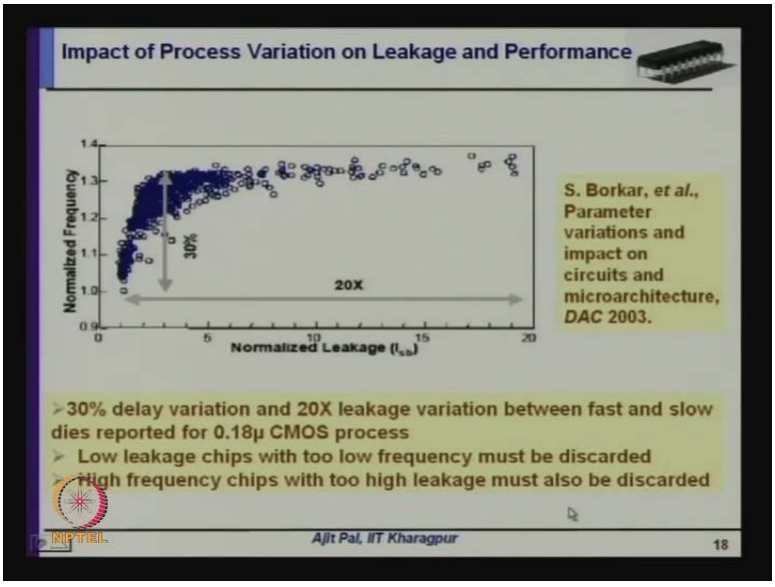

Another important factor which is becoming important that is your impact of process parameter variation as I was telling here, how the process parameter variation affects leakage and performance is shown. You can see this is taken from a paper by s broker and his colleagues they are in Intel and as you can see there is a 30 percent of delay variation here you can see the delay is varying 30 percent, one normalized frequencies here it is one and here it is 1.3. So, there is a 30 percent variation of delay for the same I c the I mean, for different chips the delay has been measured you can see for different chips the variation is this over this range 30 percent delay variation, but leakage for a power variation is much more 20 x; that means, 20 times leakage power variation is taking place for different devices manufactured by the same technology, and that too for point one eight micron technology and as you will go to smaller and smaller dimension this component will be more and more predominant.

So, low leakage chips with too low frequency must be discarded as you know you have to how do you select yield is dependent on the how many chips that is being fabricated are usable if it is slow you have to discard is if it is too leaky consuming too much power you have to discard it. So, low leakage chips with too low frequency must be discarded high frequency chip with too high leakage must be discarded and that is responsible for lower and lower yield.

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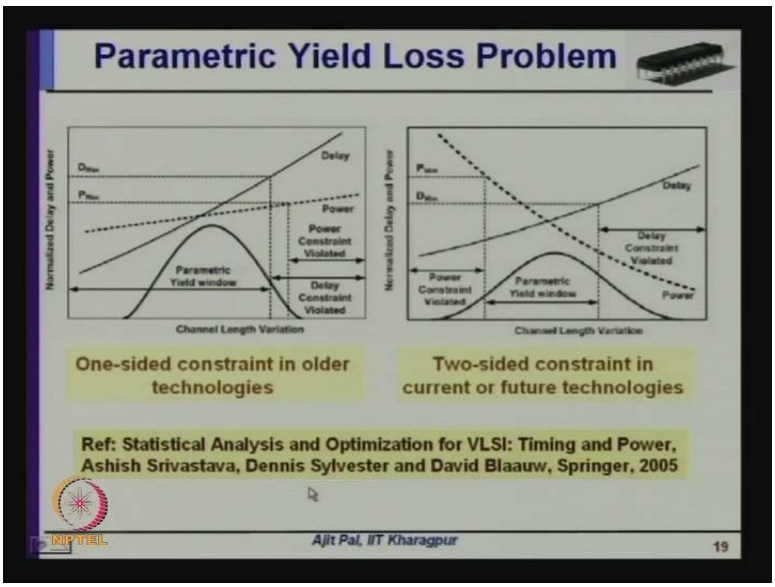

So, you have to develop techniques such that this process parameter variation is not much the circuit is process parameter variation tolerant. And particularly this is becoming important because, of this once from one-sided constraint it has shifted to two-sided constraint. You can see in the early years of VLSI circuits it was a one-sided constraint; that means, as you are reducing the channel length you can see I mean, device becoming smaller and smaller the delay was increasing I mean as you are reducing the dimension delay was reducing power dissipation was also reducing. So, you are happily going for devices of smaller and smaller dimension and that is the reason that is I mean based on this Moore's law flourished, but what has happened now a days you can see the cause of the increasing leakage power you can see as the device dimensions are reduced delay is getting reduced, but power dissipation is also increasing because of primarily because of you know that leakage power increased leakage power and as a result you have you have got a two-sided constraint. So, two-sided constraint means you have to discard the chips earlier you were discarding only these chips, but now you have to discard these chips as well as these chips. So, yield is becoming lower and lower. So, this is this is the situation of current and future technologies later on I shall discuss more about it in details and you have to use some statistical technique these parameters like channel length threshold voltage these are no longer you cannot assume them to have fixed values then now statistical parameter they vary over range with a peak at some point and on both side they reduce. So, you have to use some statistical technique to have higher yield

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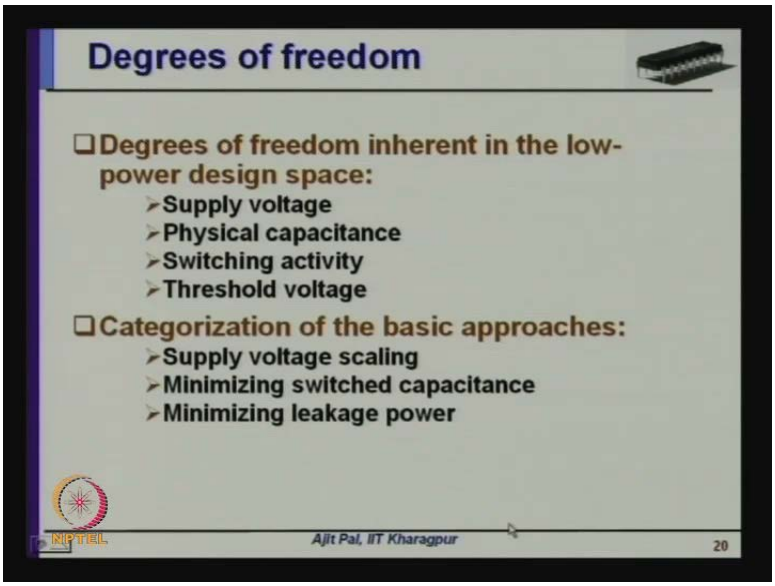

Now coming to the degrees of freedom we have to we will see that these are we have got these parameters in our hand supply voltage physical capacitance switching activity and threshold voltage these are the parameter which you have to control one or more to reduce power dissipation and based on that the basic approaches can be categorized as supply voltage scaling minimizing switched capacitance and minimizing leakage power our lecture will be organized around this we shall discuss supply voltage scaling techniques we shall discuss minimizing leakage switched capacitance how you can do that then minimizing leakage power primarily by controlling the threshold voltage.

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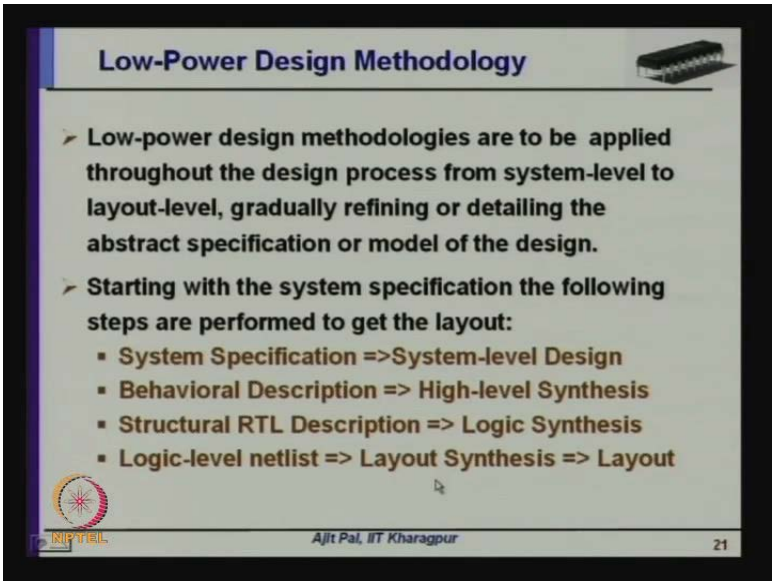

So, low-power design methodology are to be applied throughout the design process as you know it is not a single step you have got a number of steps that you have to follow in the design starting from system-level to layout-level and gradually refining or detailing the abstract specification or model of the design. So, these are the basic steps you have normally follow system specification to system-level design and then you get the behavioral description from that you get you perform high-level synthesis high-level synthesis provides you structural RTL description you use that for logic synthesis and from logic you get from logic synthesis you will get logic level net list used that for layout synthesis and finally, you will get the layout for fabrication. So, throughout this design process you have to adopt low-power design methodology

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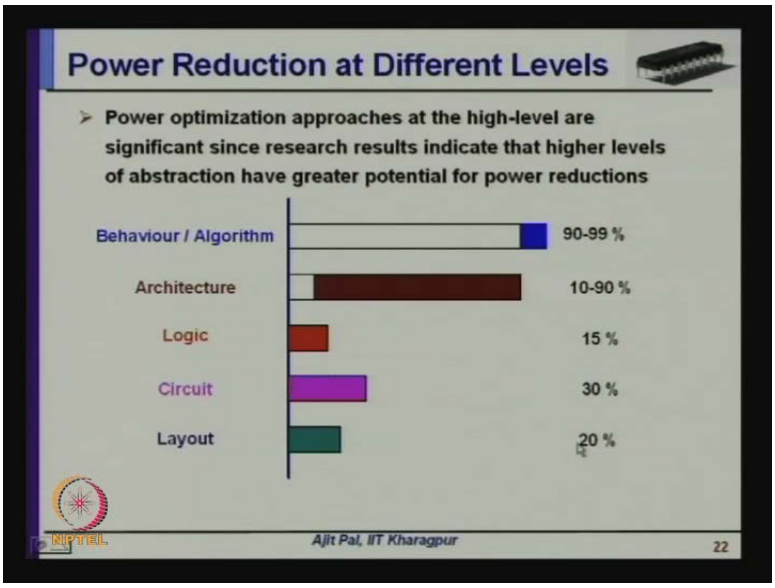

And you can see here the benefit is more and more at higher-level abstraction I mean, if you can use low-power design methodology at behavioral or level your gain can be 90 to 99 percent; that means, power dissipation can be reduced by 90 to 99 percent in the arch architectural level it can be from 10 to 90 percent, in the logic level power dissipation can be reduced by 15 percent, in the circuit level it can be reduced by 30 percent, in the layout level it can be reduced within 30 20 percent. So, you can see if you can use low-power design methodology at higher and higher level you will be more benefitted.

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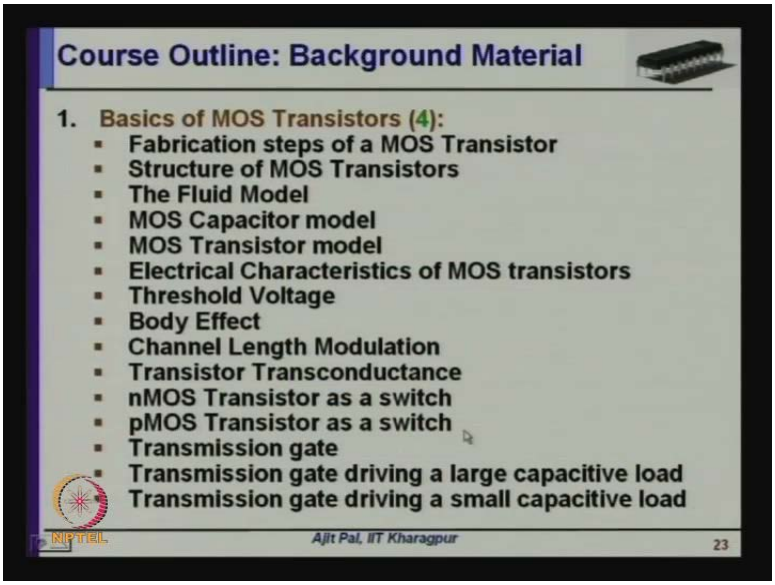

So, based on this discussion which shall be we shall we have I have developed a course outline first I shall focus on background material; that means, basics of m o s transistors 4 or 5 lectures, on basics of MOS transistors. So, I shall adopt bottom of approach starting with transistor then I shall consider invertors then I shall consider more complex circuits then systems like that.

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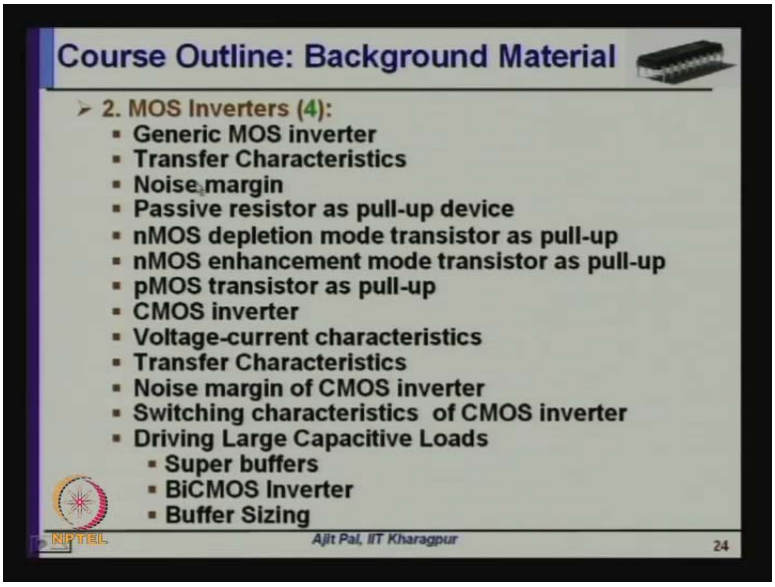

So, basics of MOS transistors followed by MOS invertors several lectures these are very various topics I shall cover in my lecture then

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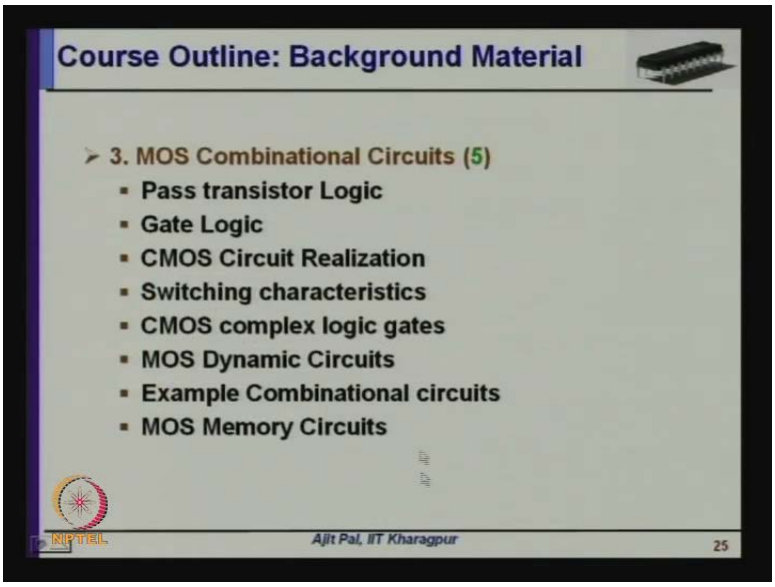

MOS combinational circuits both of I mean, combinational circuits and also MOS memory circuits I shall consider and I shall see how you can use low-power design methodology there. Then I shall switch to those lectures are essentially for developing background material. So, so that you can understand the low-power design methodology and you use them in a fruitful way.

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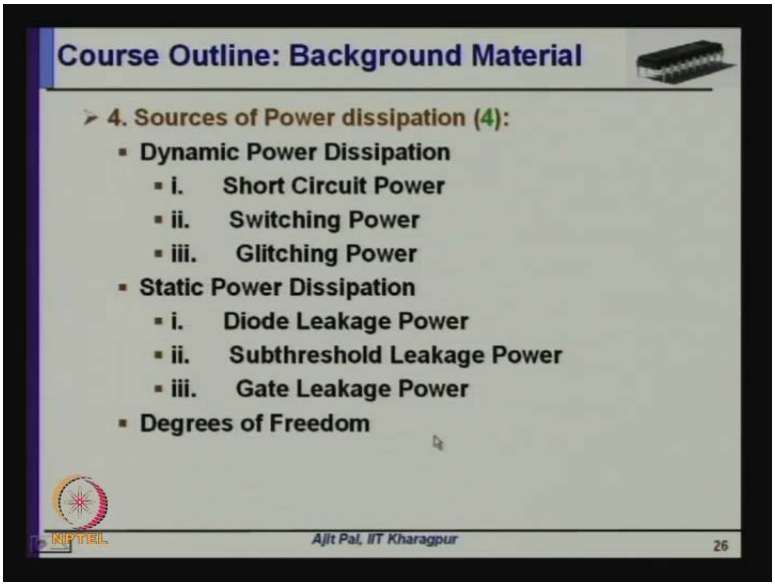

So, then comes the sources of power dissipation I should discuss in details various sources of power dissipation both dynamic and static as I told short circuit power switching power glitching power and then the various static power dissipation

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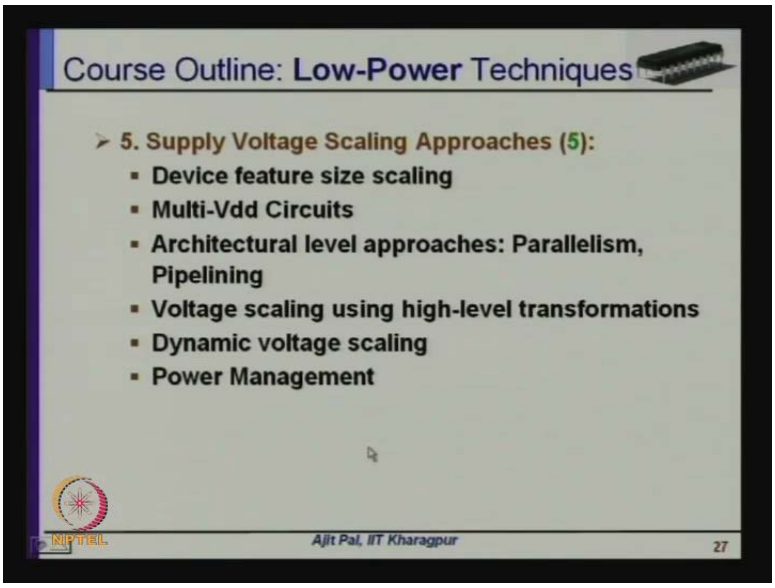

And then I shall discuss about supply voltage scaling approaches at various levels of design hierarchy. How they can be used similarly, switched capacitance minimization approaches in different levels of design hierarchy for system design then

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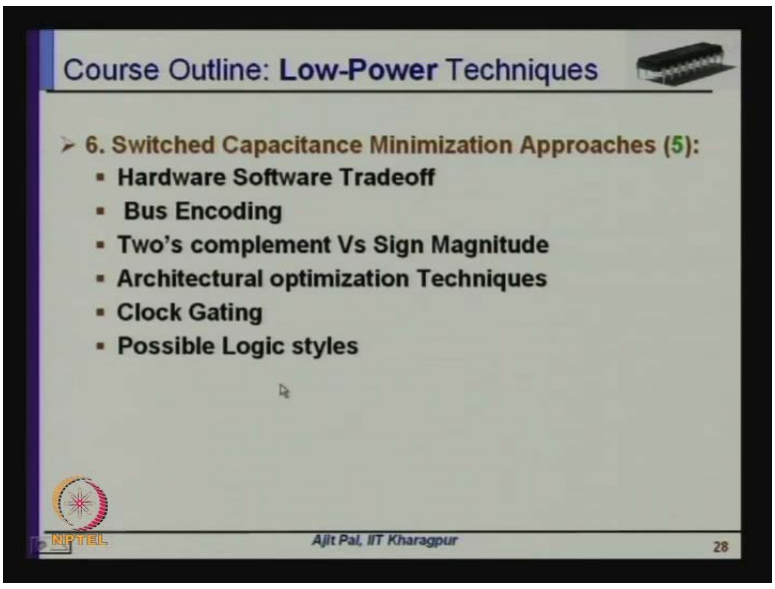

Leakage power minimization approaches at in various techniques used for leakage power minimization. Then some special topics also I shall consider like adiabatic switching circuit battery-aware synthesis variation tolerant design.

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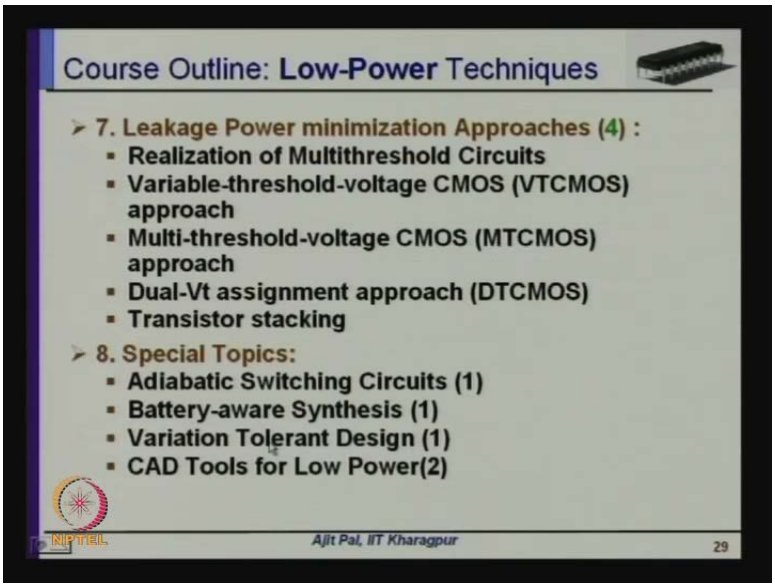

Then cad tools for lower power which is also very important. So, this is the brief outline of my lectures and with this we have come to the end of today's talk in the next lecture I shall start with m o s transistors.